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The read-out system of the ALICE pixel detector

The on-detector electronics of the ALICE silicon pixel detector includes 1200 front-end ASICs, bump-bonded to silicon sensor ladders. 5 pixel chips, mounted on a front-end bus, constitute a half-stave. The complete detector consists of 120 half-staves on two layers (see illustration). The timing, control and readout of each half-stave are done by a PILOT ASIC, mounted on a MCM together with opto-electronic transceivers. The MCM is connected to three optical fibres. The fibres carry, respectively: the incoming 40 MHz clock, the incoming trigger and configuration data, the outgoing status and readout data.

The on-detector chips have been designed in a commercial 0.25 micron CMOS technology using radiation hardening layout techniques.

The PILOT ASIC converts the incoming clock, serial trigger and serial JTAG signals into control signals for the pixel chips. The PILOT forwards the configuration data to the pixel chips, to the GOL, and to an auxiliary analog chip containing DACs that generate reference voltage and current levels. The PILOT ASIC initiates the readout of the pixel chips, converts data levels from GTL to CMOS, reformats the data stream and forwards the data to a serialiser ASIC (named GOL) that includes a driver for the laser diode transmitter. Data are sent to the control room on a fibre at 800Mb/s rate using the G-link protocol (see block digram). In the control room VME-based electronics performs zero-suppression and data encoding.
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