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VME

CORBO (RCB 8047 VME module)

User Manual
http://home.saske.sk/~ferencei/hilum/electronics/CES_RCB8047_CORBO.pdf

- Used for event counting and vetoing trigger logic while an event is being processed. It has 4 channels with one trigger input and one busy output for each.
- When it receives a trigger, it starts the BUSY. When SBC finished reading the events(readNextFragment), SBC clears the busy from Corbo, so that a new event can be read. Note that when CORBO is BUSY, it outputs a signal of 0V, when it is not BUSY, it outputs a signal of -0.8V (NIM level). So to veto a new trigger, one should input the busy signal in coincidence with the trigger, and take the output as the main trigger.
- It can communicate with SBC via interrupts or SBC polling a memory location.
- It's base address is hardcoded in ATLAS TDAQ Sofware, so one should always set it to 0x700000.
- Software can be checked out by the command:

```
source /afs/cern.ch/atlas/project/tdaq/cmt/bin/cmtsetup.sh  tdaq-05-03-00
getpkg DAQ/DataFlow/RCDExampleTriggers
```

CAEN TDC

Product page
http://www.caen.it/csite/CaenProd.jsp?parent=11&idmod=796

- Each channel can take up to 4 words. In total there is a buffer of 256 words.
- Multi Event Buffer can store up to 1024 events.
- It has a special microcontroller register, where one can do all the settings(trigger mode, reset, window width/offset)
- In our TDC (16CH) there are 2 HPTDC chips, thats why even if you have no hits, you have 6 words: Global header, HPTDC header(x2), HPTDC Trailer(x2), Global Trailer.

CAEN V792 QDC

Product page
http://www.caen.it/csite/CaenProd.jsp?idmod=41&parent=11

- Integrates voltage from detector.
- 32 channels in two 34 pin male latching IDC pin headers (Alternate ground and signal). See RibbonLemoAdapter.
- Gate signal must precede the analog input by > 15 ns
- Tolerates positive going signal up to 15 mV
- ADC counts are 1mV on storage cap. Storage cap is 100pF. Collected charge is therefore 0.1pC per count.
- 12-bit ADC gives maximum charge collection of 409.6pC
- An internal bias voltage offsets the pedestal to allow collection of small signals without clipping.
- A test on the charge/ADC relation can be seen on the elog post #219

CAEN V785 ADC

Product page
http://www.caen.it/csite/CaenProd.jsp?parent=11&idmod=285

- 16 Channel
- Up to 4V DC input range
- Minimum 10mV input
- Values above 3840 are not valid due to correction factors.

CAEN V560 Scaler/Counter

Product page
http://www.caen.it/csite/CaenProd.jsp?idmod=62&parent=11

- 16 channels
- 32-bit (~4 billion) counts

CTC VP 717 SBC

Product page
http://www.gocct.com/sheets/VP/vp71708x.htm

- VME64x
- Gigabit ethernet
- 2 x PMC slots

For access rights, see SysAdmin (restricted).

Can't log in as daquser

lnxpool41 is not connecting to LDAP, but doesn't recognize daquser.

```
Mar 23 18:28:58 lnxpool41 sshd[8713]: pam_unix(sshd:auth): check pass; user unknown
Mar 23 18:28:58 lnxpool41 sshd[8713]: pam_succeed_if(sshd:auth): error retrieving information abo
Mar 23 18:29:00 lnxpool41 sshd[8713]: Failed password for invalid user daquser from 188.184.71.39
```

LDAP not connecting

SysAdmin ticket
https://atd-sysadmins.cern.ch/redmine/issues/4295

```
Mar 23 17:33:01 lnxpool41 sudo: pam_ldap: ldap_simple_bind Can't contact LDAP server
Mar 23 17:33:01 lnxpool41 sudo: pam_ldap: reconnecting to LDAP server...
Mar 23 17:33:01 lnxpool41 sudo: pam_ldap: ldap_simple_bind Can't contact LDAP server
```

CMEM_RCC initilisation error:

Getting the following message in the kernel boot log.

```
Mar 23 15:33:07 lnxpool41 kernel: cmem_rcc(cmem_rcc_init): Failed to determine the BPA base addre
Mar 23 15:33:07 lnxpool41 kernel: cmem_rcc(cmem_rcc_init): Check if BPA memory has been reserved
```

Error message - throwing the following error on login:

On lnxpool41

```
TDAQ drivers errors during boot:
Error: /Stage[main]/Tdaq::Drivers/Exec[/bin/atlas_tdaq_drivers load]/returns: change from notrun

Other Puppet errors during boot:
Error: /bin/atlas_tdaq_drivers load returned 1 instead of one of [0]



Mon Mar 23 15:33:14 CET 2015 BWMboot2 failed r=6
```

Probably related to the cmem_rcc error above.

Login problem - throwing the following error on login:

On lnxpool41

```
TDAQ drivers errors during boot:

Other Puppet errors during boot:
Error: /Stage[main]/Bwm::Mntbwm/Mount[/mnt/bwm]: Failed to call refresh: Execution of '/bin/umoun
Error: /Stage[main]/Bwm::Mntbwm/Mount[/mnt/bwm]: Execution of '/bin/umount /mnt/bwm' returned 16:



Wed Mar 18 17:22:48 CET 2015 BWMboot2 failed r=6

Connection closed by 137.138.89.85
```

Problem disappeared after testbed system reset. - Not understood.

Continuous console message:

On sbctest-717

```
intel ips 0000:00:1f.6: MCP limit exceeded: Avg power 48000, limit 18000
```

Bug report on launchpad
https://bugs.launchpad.net/ubuntu/+source/linux/+bug/636045

Suggestions are to blacklist the intel_ips kernel module, or to filter these messages from syslog. Information from the module is in

```
/sys/kernel/debug/ips/
```

It would be interesting to understand why sbctest-717 shows this error while lnxpool41 does not.

VME crate (Wiener UEV 6021-LHC6U-VME-Bin)

Product page
http://www.wiener-d.com/sc/powered-crates/vme/6u-vme-6021.html

Fan tray (Wiener UEL 6020 A)

Power supply (Wiener UEP 6021)

PCs

For access rights, see SysAdmin (restricted).

Operating systems

SLC6

Linux installation at CERN

Microsoft Windows

Installation of Windows at CERN

Testgear

Tektronix TDS 2024B DSO

Product page
http://www.tek.com/oscilloscope/tds2000-digital-storage-oscilloscope

- 4 channel
- 200 MHz bandwidth
- 2 GSamples per second

From the manual:

> The oscilloscope inputs do not properly terminate low impedance cabling. To avoid amplitude inaccuracy from improper loading and reflections, place a 75 ohm feedthrough terminator (Tektronix part number 011-0055-02 or equivalent) between the 75 ohm coaxial cable from the signal source and the oscilloscope BNC input.

USB TMC control

TTI TG5011 Arbitrary pulse generator

Manual
https://aismisc.cern.ch/aismisc/ess.file_utils.download_pooldoc_file?pooldoc_id_in=4458

This unit was used for testing the DelayWireChamber and general testing of other hardware. For the DWC, check the output voltage is 40 mV peak-to-peak. A 10kHz frequency is fine and the pulse should be ~40ns. Unfortunately the rise time + fall time must be less than or equal to the pulse width.

Note - this unit has a USB com port interface.

-- CenkYildiz - 14 Mar 2014

This topic: BL4S > DaqHardware
Topic revision: r19 - 2015-09-07 - TimBrooks