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# DESY 2017-06 ECAL "10 SLABs"

Test 10 Short SLAB's in flexible frame, at DESY.

This page is a copy of SiWCERN201511. It can be edited by the members of the SiWDESY201706Group .

## Organisation

### Responsibilities & Contacts

Contacts admin Vincent Boudry +33 6 7131 0577,

Coordinator: Adrián Irlés

Technical Coordinator: Frédéric Magniette

e-group of TB-participants: SIWECAL-BT2017@cernNOSPAMPLEASE.ch ( Management link [↗](#))

Elog [↗](#)

## Docs

- Main Page (Twiki) "Old" Page (Forge IN2P3) [↗](#)
- DESY Beam test Area
- CERN2015 Shift Instructions
- DESY page of AIDA-2020 TNA [↗](#)
  - ◆ condition for travel and stay reimbursement [↗](#)
- **MANDATORY**
- DESY Beam test safety Instructions [↗](#)
- DesyAccessCard

### Lodging:

- The DESY Hostel [↗](#) is available by sending a mail or by registering online [↗](#)

## Pre-Expedition planning

### Planning

- Availability: Doodle [↗](#)
- Planning of presence [↗](#) (google sheet)
- tentative Schift schedule: (google sheet) [↗](#)

## Materials & Logistics

## Talks, proceedings and papers

Articles and Proceedings Repository: <https://github.com/SiWECAL-TestBeam/TB2017-doc/> [↗](#)

- Commissioning document, submitted to arxiv: <https://arxiv.org/abs/1810.05133>
  - ◆ Figures and tex document are in:  
<https://github.com/SiWECAL-TestBeam/TB2017-doc/tree/master/performance-paper-draft/commissioning>
- Commissioning & Beam Test Performance paper, submitted to NIMA and arxiv:  
<https://arxiv.org/abs/1902.00110>
  - ◆ Figures and tex document are in:  
[https://github.com/SiWECAL-TestBeam/TB2017-doc/tree/master/performance-paper-draft/NIMsub\\_a](https://github.com/SiWECAL-TestBeam/TB2017-doc/tree/master/performance-paper-draft/NIMsub_a)

## Conferences

- Calice Meeting Mainz 2018
  - ◆ Analysis of BT2017: <https://agenda.linearcollider.org/event/7798/contributions/41030/>
- Calice Meeting at Tokyo, September 2017:
  - ◆ TB performance: <https://agenda.linearcollider.org/event/7630/contributions/39768/>
  - ◆ Mechanical structures: <https://agenda.linearcollider.org/event/7630/contributions/39772/>
- CHEF2017:
  - ◆ TB performance: <https://indico.cern.ch/event/629521/contributions/2703010/>
    - ◇ Open Acces proceeding: <https://arxiv.org/abs/1802.08806>
  - ◆ Pyrame3: <https://indico.cern.ch/event/629521/contributions/2703025/>
    - ◇ Proceeding <http://inspirehep.net/record/1662010>
  - ◆ Sk2 & SK2a performance <https://indico.cern.ch/event/629521/contributions/2703017/>
    - ◇ O.A. proceeding: <https://arxiv.org/abs/1801.02024>
- LCWS 2017:
  - ◆ TB performance <https://agenda.linearcollider.org/event/7645/contributions/39935/>
    - ◇ Proceeding ?
- IEEE 2017:
  - ◆ The SiW -ECAL technological prototype (poster) (see attachment [https://twiki.cern.ch/twiki/pub/CALICE/SiWDESY201706/poster\\_v6.pdf](https://twiki.cern.ch/twiki/pub/CALICE/SiWDESY201706/poster_v6.pdf))
    - ◇ O.A. proceeding: <https://arxiv.org/abs/1801.10407>

## Commissioning

### Beam test area

## Hardware status and detector configuration

### Slabs

Information about the slabs is in <https://forge.in2p3.fr/projects/calice/wiki/Si-WEcalSLABS>

For example, if one looks into <https://forge.in2p3.fr/projects/calice/wiki/SiWEcalSlab13> will see:

sU\_4b\_11\_F\_#13

FEV11 n°33

SMBV4b n°11

Then, the PCB n° 33, corresponds to the row 5 of the table table, and the wafers Wafers n° 10 13 15 14

There is also an ASU table (PCB+Wafer) <https://forge.in2p3.fr/projects/calice/wiki/Si-WEcalASU>

## Settings

Spill settings: 5Hz, 3.7ms width: 0.9 (start acq) + 0.5 (val evt) + 2.3 ms (real spill) Trigger thresholds: >230 for all chips (set in the commissioning procedure). Choice done chip-wise. Standard acquisition: 30 minutes per point.

Some re-masking of single channels has been done during the calibration. The final xml configuration file is used for all the other runs (showers, angle, magnet) with no further changes.

- SETUP:

	A	B	C	D	E
1	<b>Layer</b>	<b>SLAB</b>	<b>LV cables/connectors</b>	<b>LV PS</b>	<b>HV cables/conn</b>
2	<b>1</b>	21	1	1	5
3	<b>2</b>	16	2	1	5
4	<b>3</b>	17	3	1	6
5	<b>4</b>	18	4	1	6
6	<b>5</b>	19	5	1	6
7	<b>6</b>	20	6	2	7
8	<b>7</b>	22	7	2	7
9					

The slab ordering shown above was kept unchanged for all the testbeam except at the end, when the first layer was moved out from the beginning of the detector to the other beam area, TB24/2 with the PCMag.

Summary of masked channels: Total # of channels not masked --> 6204 (87%)

Layer 1, Slab 21 43.4% (one wafer) Layer 2 6, slabs 16,-20 ~6-8% Layer 7, slab 22, ~ 16% (one chip)

5% are masked manually just before starting the commissioning same patten in all slabs: Chn 37 in all chips, Chn 41-53, chips 1,9 Chn 5, chips 0 and 8 Chn 3, 9, 10, chip 7 and 15

The trigger threshold were set chip-wise as the maximum of the scurve threshold + 5 sigmas or 225 DAC.

## Physics program

The data taking program consisted in the MIP calibration using 3GeV positrons, the shower using different energy positrons and different width of tungsten between the slabs, a mip run with the detector in an angle of ~45 degrees with respect the beam and a set of runs of single slab (21) inside the magnetic field.

### MIP calibration using positrons

Shower Program

Magnetic field tests

MIPs at 45 degrees

Slabs

## Analysis

Check the page above for analysis tools and the dedicated BT analysis internal meetings:  
<https://indico.in2p3.fr/category/652/>

## Pictures

-- VincentBoudry - 2017-06

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This topic: CALICE > SiWDESY201706

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