

**Silicon pixel-detector R&D for CLIC**

- Speaker: Magdalena Munker (CERN)
- Status: Accepted
- Abstract: The silicon vertex and tracking detectors at the CLIC multi-TeV linear e+e- collider must have excellent spatial resolution, full geometrical coverage extending to low polar angles, extremely low mass, low occupancy facilitated by time-tagging, and sufficient heat removal from sensors and readout. These considerations, together with the precision physics needs and beam structure of CLIC, push the technological requirements to the limits. A detector concept based on hybrid pixel technology is under development for the CLIC vertex detector, profiting from synergy with detectors developed for imaging applications. Timepix and Timepix3 readout ASICs are used as technology platforms for the evaluation of ultra-thin (50-300 micron) slim-edge and active-edge sensors. The CLICpix chip was derived from the Medipix/Timepix architecture as a small-pitch (25 micron) readout ASIC implemented in 65 nm CMOS technology. It comprises fast time stamping (~10 ns) and can be operated in pulsed powering mode, to reduce the average power consumption to a level compatible with cooling through forced air flow (<50 mW/cm<sup>2</sup>). Charge interpolation between neighbouring pixels results in a single-point resolution of a few micron. Prototype assemblies of CLICpix ASICs bump bonded to planar sensors or capacitively coupled to active HV-CMOS sensors have been tested successfully with radioactive sources and in test beams. For the outer tracking region, both hybrid concepts and fully integrated CMOS sensors are under consideration. Seamless tiling of sensors in large areas requires the use of Through-Silicon-Via (TSV) technology. A TSV process was therefore developed for Medipix3 and thinned (50 microns) Timepix3 ASICs, in collaboration with Medipix and external partners. This talk gives an overview of the R&D program for silicon detectors at CLIC.
- slides

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This topic: CLIC > IWoRiD

Topic revision: r3 - 2016-07-08 - EvaSicking



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