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iWoRiD 2017

Abstracts

The test beam results of SOI pixel detector

- Speaker: Roma Dasgupta, Marek Idzik (AGH-University of Science and Technology)
- Status: Oral presentation (20 min)
- Abstract: The Silicon-On-Insulator (SOI) CMOS technology implements the insulator (silicon dioxide) between the handle wafer and the silicon layer with electronics. This feature allows to design monolithic pixel detectors without bump-bonding. Reduction of detector thickness limits particle scattering which results in a better spatial resolution. This is a significant advantage for vertex and tracking detectors at future linear colliders. A prototype of a SOI pixel detector was designed in Cracow and fabricated in Lapis 200 nm SOI CMOS technology. In June-August 2016 it was for the first time tested in the test beam at the CERN SPS H6 beamline. In this contribution the results of this test beam campaign are presented. The tested detector is produced on 500 um thick high resistivity floating zone wafer. The pixel architecture is based on source-follower and pixel size is 30x30 um. The analysis procedure includes pedestal and noise calculation, correlation with the CLICdp Timepix3 reference telescope, different cluster reconstruction algorithms, as well as alignment and eta correction. Current results give a spatial resolution of about 4 um in both X and Y directions.
  The spatial resolution is presented as a function of the back bias voltage. Moreover, a detector efficiency was calculated and the preliminary results show almost 99%.
- Slides

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