Table of Contents

Lab testing procedure (CLICpix+CCPDv3)

For all work with the clicpix + hv-cmos assemblies, care should be taken not to turn on the FPGA board directly after turning it off. Doing so will cause the chip to burn like an LED and self-destruct. This is not a joke.

To set up the system from scratch, navigate to the folder /home/pixel/uASIC/software/trunk and source the setup script env.sh. Make sure that control hub is running by running the start command: sudo /opt/cactus/bin/controlhub_start. To start up the hardware, connect the FPGA via ethernet cable to the computer, and make sure that the computer port IP is set to 192.168.200.1. Then turn on the FPGA and check (after a few seconds) that it responds by pinging it at 192.168.200.16.

Quick electrical test (CLICpix+CCPDv3)

The first test of the assembly should be to make sure there are no shorts on the PCB/bond wires. This is performed as follows:

- Plug the assembly into the interface board (while the FPGA is powered off)
- Turn on the FPGA and make sure that you can ping it
- Run the script ccpd_test.py

The script will set the voltage regulator output and read back the voltages and currents. Check that the voltage is correctly set, and look at the currents. In general if these reach 100-200 mA then turn off the system quickly! If testing a system for the first time, look and record the current values on DACs 3, 4 and 5, saving the results in CurrentsHVCMOS.txt.

IV Measurement (all types of assemblies)

The next check is to make sure that there is no problem with the high voltage. In the lab there is a keithley which can be connected to the computer via ethernet cable. Check the IP on the keithley and put this value into the script iv.py. To perform the measurement:

- Plug the high voltage into the LEMO connector on the interface board (if in doubt, ask!)
- Cover the sensor with foam/something to prevent light from falling on the sensor
- Run the script iv.py to record the IV curve
- Turn off the high voltage
- The output data is stored by default in /storage/pixel/data/hvcmos_iv/"current time and date" - rename this to the assembly name
- Plot the IV curve using the script /storage/pixel/data/hvcmos_iv/plotIV.gnu, after changing the title, input path and output path
- Upload the IV curve to the table below

The CCPDv3 sensor should show a sharp increase in current at 93 V, but in general should be lower than approximately 50 nA.

CLICpix test

This is the first test to check the response of the CLICpix and to see that it is operational/usable. It consists of two steps: threshold equalisation of the pixel matrix and a threshold scan. This threshold scan can be used to determine the operating point of the device. To perform the test:

- Bias the HV-CMOS to -60 V (making sure that the sensor is dark)
- Run the script clicpix_eqalize.py with options "-e -s -n" (equalise, threshold scan, negative polarity)
- Turn off the high voltage
- The threshold scan plots, ScanActivePixels.png and ScanPixelCount.png, should be output by default to /home/pixel/uASIC/software/trunk/data/BOARD_ID/equalization/DATA_AND_TIME - upload to the table below

HV-CMOS (CCPDv3) test

Now that the CLICpix is responding, the final check is that the HV-CMOS is also working. An indication of this should be given by the electrical tests above - the current consumption for DAC 3 should be of order 45 mA. Before taking any data, the operating threshold of the CLICpix must be determined. This can be done by looking at the threshold scan plots from the previous test - pick a value of the threshold for which the number of pixels responding is small (order 40-50). This should be approximately 120 DAC steps from the equalisation mean. Then:

- Edit the script radsource.py to include the threshold for this device
- Turn on the high voltage
- Without a source on top run the radsource.py script and observe the number of counts per frame. If this is >> 200 then reduce the threshold DAC and try again
- Once the threshold doesn't produce too many noise hits, take data by running radsource.py with argument "WithoutSource". This will produce the output file frames/chipIDXXX.

Now the test should be performed again with a source on top of the HV-CMOS. Take the Sr90 source from the safe (remembering to display the source card next to the setup)

- Place the source on top of the HV-CMOS
- Run the script radsource.py with argument "WithSource" and observe the number of counts (should be noticeably higher)

It is possible that on the first attempt the source will not be completely aligned with the sensor. In this case, repeat the measurement while moving the source until you find the maximum number of counts. Then take one set of data without moving the source further.

CLICpix2 tests

- Lab elog

CLICTD Tests

Bias voltages are applied to the p-wells and the substrate of CLICTD. There are two possibilities to apply the voltage:

- Directly on the PCB: allows the p-well and substrate to be biased individually. To use this mode, place the two red jumpers at the second row (closer to the margin of the board) such that the central pin is not covered.
- From the CarBoard: the same bias voltage is applied to p-well and substrate. To use this mode, place one jumper on the second row such that the central pin and one neighbour (either left or right) is covered. The second jumper is placed on the first row such that the central pin and the neighbouring pin are covered (if left neighbour in second row is covered, right neighbour in first row need to be covered and vice versa).

Assembly results

Type	Assembly	Board ID	Description	Status	Tests performed	IV plot	Thre sc cou p
CCPDv3	SET9	001ec0db94b1	Ideal alignment	Alive in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET10	001ec0db2e5e	Quarter pixel misalignment	Alive in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET11	001ec0dafabc	Half pixel misalignment	Unresponsive (?) in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET12	001ec0dbabb9	Ideal alignment, thicker glue	Alive in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET13	001ec0db2082	Ideal alignment	Alive in beam area	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET14	001ec0db5bfb	Half pixel misalignment	Alive in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET15	001ec0db5ca6	Ideal alignment, thicker glue	Alive in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CCPDv3	SET16	001ec0db5ca6	Half pixel misalignment	Alive in lab	Electrical, IV, CLICpix	IV curve	Thre scan
CLICTD	A1	-	Modified process with continuous n-type implant	Alive in lab	IV, Equalisation, Source and xray measurements	-	-
CLICTD	A2	-	Modified process with continuous n-type implant	Broken	Equalisation, xray measurements	-	-
CLICTD	A3	-	Modified process with continuous n-type	Broken	-	-	-

			implant				
CLICTD	A4	-	Modified process with continuous n-type implant	Alive in lab	Equalisation	-	-
CLICTD	A5	-	Modified process with continuous n-type implant	Broken	-	-	-
CLICTD	A6	-	Modified process with continuous n-type implant	Alive in lab	-	-	-
CLICTD	A7	-	Modified process with continuous n-type implant	Alive in lab	-	-	-
CLICTD	A8	-	Modified process with continuous n-type implant	Broken	-	-	-
CLICTD	A9	-	Modified process with continuous n-type implant	Alive in lab	-	-	-
CLICTD	A10	-	Modified process with continuous n-type implant	Alive in lab	-	-	-
CLICTD	B1	-	Modified process with gap in n-type implant	Broken	IV, Equalisation, Source and xray measurements	-	-
CLICTD	B2	-	Modified process with gap in n-type implant	Alive in lab	Equalisation, xray measurements	-	-
CLICTD	B3	-	Modified process with gap in n-type implant	Broken	-	-	-
CLICTD	B4	-	Modified process with gap in n-type implant	Alive in lab	Equalisation	-	-

CLICTD	B5	-	Modified process with gap in n-type implant	Alive in lab	-	-	-
CLICTD	B6	-	Modified process with gap in n-type implant	Alive in lab	-	-	-
CLICTD	B7	-	Modified process with gap in n-type implant	Alive in lab	-	-	-
CLICTD	B9	-	Modified process with gap in n-type implant	Alive in lab	-	-	-
CLICTD	B10	-	Modified process with gap in n-type implant	Alive in lab	-	-	-
CLICTD	W18_1	-	Cz / high dose / extra p-well	Alive in lab	-	-	-
CLICTD	W15_1	-	Cz / intermediate dose / gap	physically damaged / scratch	-	-	-
CLICTD	W8_1	-	Epi / low dose / extra p-well	IV good, no configuration	-	-	-
CLICpix+planar	43 W	001ec0da56b4	worst planar sensor	Alive in lab	Electrical, IV, CLICpix	IV curve	Thres scan
CLICpix+planar	14 ok	001ec0da4e0d	ok planar sensor	Alive in lab	Electrical, IV, CLICpix	IV curve	Thres scan
CLICpix+planar	31 best	001ec0da578c	best planar sensor	Alive in lab	Electrical, IV, CLICpix	IV curve	Thres scan
CLICpix+planar	50um-4	001ec0dacbb6	Active edge 50um thick	Alive in lab	Electrical, IV, CLICpix	IV Curve	Thres scan
CLICpix+planar	150um-6	001ec0dab10e	Active edge 150um thick	Alive in lab	Electrical, IV, CLICpix	IV Curve	Thres scan
CLICpix2+planar	11-FBK398-1 (assembly 14)		FBK act. edge 130 um thick, n-in-p	Alive, nominal threshold = 1250 , nominal bias = -60V, baseline from lab equalisation = 1200 , half of matrix unconnected	equalised, TP, source meas., test-beam data taken at SPS	IV Curve	

CLICpix2+planar	9-ADV100-4 (assembly 9)		Advacam act. edge 100 um thick, GR GND, n-in-p	Alive, bonding problems found		IV Curve	
CLICpix2+planar	15-ADV150-9 (assembly 15)		Advacam act. edge 150 um thick, GR GND, n-in-p	Alive, bonding problems found		IV Curve	
CLICpix2+planar	3-FBK398-2 (assembly 16)		FBK act. edge 130 um thick, n-in-p	Alive, nominal threshold = 1190, nominal bias = -60V, baseline from lab equalisation = 1148	equalised, TP, source meas., test-beam data taken at SPS	IV Curve	
CLICpix2+planar	ADV-S5 (assembly 18)		Advacam act. edge 100 um thick, no GR, Ni/Au UBM, n-in-p	Unresponsive after bias applied, thought to be because of the ASIC damage		IV Curve	
CLICpix2+planar	FBK398-3 (assembly 19)		FBK act. edge 130 um thick, n-in-p	Alive, nominal threshold = 1190, nominal bias = -60V, baseline from lab equalisation = 1111	equalised, TP, source meas., test-beam data taken at DESY	IV Curve	
CLICpix2+planar	FBK398-4 (assembly 20)		FBK act. edge 130 um thick, n-in-p	Alive, nominal threshold = 1290, nominal bias = -60V, baseline from lab equlaisation = 1243	equalised, TP, source meas., test-beam data taken at DESY	IV Curve	
CLICpix2+planar	ADV-S3 (assembly 21)		Advacam 100 um thick, Ni/Au	Alive in lab, nominal bias -50V, nominal threshold 1285, baseline in lab equalisation = 1184. Large short region discovered in centre and at one edge of the pixel	configured, IV scan, equalised, source measurement, TP measurement, categorisation	IV CurveIV Curve (new)	

				matrix (see pixel categorisation plot).			
CLICpix2+planar	ADV-S2 (assembly 22)		Advacam 50 um thick, Pt	Can be configured but draws high current. Can be operated up to -1.8V before hitting current limit of 100uA. Operational voltage of -0.4V with 146 masked pixels for low noise at a threshold of 1335 (current ~20uA), baseline from lab equalisation = 1183. Could only be equlaised with no bias applied. Fragile.	configured, equalised at 0V only, IV scan, test pulsing, response to source in noise level therefore cannot be seen. Going to DESY test beam.	IV Curve (powered) IV Curve (unpowered) IV Curve (forward bias)	
CLICpix2+planar act.edge	FBK-3826-C7-A5		FBK 130 um thick, active edge	alive in lab	operation up to ~60V (@~65-80uA), can be equalised, responds to Sr90	I/V curve (unpowered)	
CLICpix2+planar act.edge	FBK-3826-C4-B4		FBK 130 um thick, active edge	alive in lab	operation up to ~80V (@~1uA), can be equalised	I/V curve (unpowered)	
FASTPix	W03-S1-1	-	Not optimised flavour	Alive in lab	Test-Beam Data	-	-
FASTPix	W15-S1-1	-	Optimised flavour with low-dose nx	Alive in lab, very noisy	Test-Beam Data	-	-
FASTPix	W15-S1-2	-	Optimised flavour with low-dose nx	???	???	-	-
FASTPix	W15-S1-3	-	Optimised flavour with low-dose nx	???	???	-	-
FASTPix	W18-S1-1	-		Alive in lab		-	-

			Optimised flavour with high-dose nx		Test-Beam Data		
FASTPix	W18-S1-2	-	Optimised flavour with high-dose nx	???	???	-	-
FASTPix	W18-S1-3	-	Optimised flavour with high-dose nx	???	???	-	-
FASTPix	W18-S1-4	-	Optimised flavour with high-dose nx	???	???	-	-
FASTPix	W18-S1-5	-	Optimised flavour with high-dose nx	???	???	-	-
DPTS	???-40-1	-	Chip #40 DPTS (base version)	Alive in lab	???	-	-
DPTS	???-40-2	-	Chip #40 DPTS (base version)	Alive in lab	???	-	-
DPTS	???-45-1	-	Chip #45 DPTS-X (change in the encoding to reduce charge sharing)	Alive in lab	???	-	-
DPTS	???-45-2	-	Chip #45 DPTS-X (change in the encoding to reduce charge sharing)	Alive in lab	???	-	-

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