

RO Mappings for TB November 2011

ADC0 (before run 6287)	
Readout Channel	Signal
ADC0-1	newDREAM S1
ADC0-2	newDREAM S2
ADC0-3	newDREAM S3
ADC0-4	newDREAM S4

ADC0 (after run 6287)	
Readout Channel	Signal
ADC0-1	newDREAM C2
ADC0-2	newDREAM C3
ADC0-3	newDREAM C4
ADC0-4	newDREAM C1
ADC0-6	newDREAM S1
ADC0-7	newDREAM S2
ADC0-8	newDREAM S3
ADC0-9	newDREAM S4

ADC1	
	(after run 6287 it is empty)
Readout Channel	Signal
ADC1-1	newDREAM C1
ADC1-2	newDREAM C2
ADC1-3	newDREAM C3
ADC1-4	newDREAM C4

ADC2		
Readout Channel	Signal	
ADC2-0	L1	Neutron15
ADC2-1	L2	Neutron13
ADC2-2	L3	Neutron1
ADC2-3	L4	Neutron2
ADC2-4	L5	Neutron3
ADC2-5	L6	Neutron4
ADC2-6	L7	Neutron12
ADC2-7	L8	Neutron9
ADC2-8	L9	Neutron10
ADC2-9	L10	Neutron11
ADC2-10	L11	Neutron14
ADC2-11	L12	Neutron8
ADC2-12	L13	Neutron5
ADC2-13	L14	Neutron16
ADC2-14	L15	Neutron7
ADC2-15	L16	Neutron6

ADC3 (multigate)			
Readout Channel	Signal	Readout Channel	Signal
ADC3-1	PS	ADC3-12	H1-LD1
ADC3-9	T3	ADC3-13	H1-LD2
ADC3-10	TC	ADC3-14	H1-LD3
ADC3-11	mu	ADC3-15	H1-LD4

TDC							
Readout Channel	Signal	Readout Channel	Signal	Readout Channel	Signal	Readout Channel	Signal
TDC-0	DWC1-Left (BC1)	TDC-4	DWC2-Left (BC5)	TDC-8	H1-1	TDC-12	H1-5
TDC-1	DWC1-Right (BC2)	TDC-5	DWC2-Right (BC6)	TDC-9	H1-2	TDC-13	H1-6
TDC-2	DWC1-Up (BC3)	TDC-6	DWC2-Up (BC7)	TDC-10	H1-3	TDC-14	H1-7
TDC-3	DWC1-Down (BC4)	TDC-7	DWC2-Down (BC8)	TDC-11	H1-4	TDC-15	H1-8

DRS					
DRS Channel	CableName	Signal	DRS Channel	CableName	Signal
gr0-0	X1	Xtal1 - Q1 Franco	gr2-0	X8	Xtal1
gr0-1	X2	Xtal2- Q2 Franco	gr2-1	X9	Xtal2
gr0-2	X3	Xtal3- S1 Franco	gr2-2	X10	Xtal3
gr0-3	X4	Xtal4- S2 Franco	gr2-3	X11	Xtal4
gr0-4	X5	Xtal5	gr2-4	X12	Xtal5
gr0-5	X6	Xtal8	gr2-5	X13	Xtal8
gr0-6	X7	Xtal9	gr2-6	X14	Xtal9
gr0-7	empty		gr2-7	empty	
gr0-8	trigger		gr2-8	trigger	

-- SilviaFranchino - 05-Nov-2011 -- MicheleCascella - 06-Nov-2011

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