-- JeanPierreCachemiche - 27 Sep 2007

Procedure

For all the operations below, you must first log on the CERN gateway (**lbgw.cern.ch** if you are outside from CERN or **gw01.cern.ch** if you are at CERN), and from there on the local master (**tmudaq01**) using Pierre-Yves Duval account (see him for user name and password).

By default the FPGAs are programmed with the operational version of the code that **includes the required functionality** starting from version 0.6 of the BCSU code. If an earlier version is programmed in the Flash EEPROMs, it is necessary to load the BCSU_V_0.6 firmware in the FPGAs memories. The procedure is the following:

Start a run on the TFC

Configure the TFC and start a run (this must be done before beginning the next steps).

NB : if you want to use a periodic trigger, pause the run in order to **disable the L0-accepts** for the next steps.

Program the L0Muon processor

Configure the BCSUs (load the config (.pof/sof) in the FPGA)

Launch the TOOLBOX utility available trough PVSS to be able to program the FPGAS of a crate through the ECS.

- Select the crate by ticking the appropriate crate case at the top of the screen;
- Select the processing boards by ticking the cases 0 to 11;
- Click on the Command list button at the bottom of the screen;
- Double click on *BCSU_Load_Ram* : the command is dispayed in the caption at the bottom of the page;
- Click on the Send Parallel CMD button to launch the command in parallel on all the processing boards;
- At this time the a yellow led is highlighted in front of each board during the whole duration of the programming (approximately 5 minutes);
- When the programming is over, the yellow led turns to blue for each board : at this time all the processing boards are programmed.

Program the BCSUs (set the BCSU registers for the test)

Launch the TOOLBOX utility available trough PVSS to be able to program the FPGAS of a crate through the ECS (if not done already).

- Select the crate by ticking the appropriate crate case at the top of the screen;
- Select the processing boards by ticking the cases 0 to 11 (short cut : use the all button);
- Click on the *Command list* button at the bottom of the screen;
- Double click on *_Send_Sim_L0_Data_to_TELL1* test : the command is dispayed in the caption at the bottom of the page;
- Click on the *Send Parallel CMD* button to launch the command in parallel on all the processing boards;
- At this time the a yellow led is highlighted in front of each board during the execution of the command (a few seconds);
- When the command execution is finished, the yellow led turns to blue for each board : at this time all the BCSUs emit the pattern described below.

Program the controller board (set the CU registers for the test)

Launch the TOOLBOX utility available trough PVSS to be able to program the FPGAS of a crate through the ECS (if not done already).

- Select the controller board by ticking the appropriate crate case;
- type (and send) the command _Send_BC0_reset_at_BC3464

Configure the TELL1

Here is an example of an operationnal TELL1 configuration file : RICH1.v21.cfg.EXTtrig

Note that only one out of 4 GigaBit ehernet was used for the output. All input optical links were activated. Rate up to 1 L0Accept per orbit was sustain.

Send triggers

If you have programmed the TFC to send periodic trigger and have paused the run : it's now time to continue the run. You can also sent single shot triggers.

What the program does

This program sends simulated L0 derandomizer data to the TELL1 board.

The program uses external broadcast signals coming from the controller board. PU data are built by an embedded PU emulator inside the BCSU. This simulator is reset on every BCreset received from the controller board.

The PU simulator builds continuously candidates that are selected by the BCSU. From these candidates the BCSU enters information in the L0 buffer. Each time a L0_Accept is received the corresponding candidate is entered in the L0 derandomizer.

In parallel, the PU simulator builds simulated L0 derandomizer informations that are emitted on every L0_Accept received from the controller board.

The PU and BCSU L0 derandomizer information are concatenated to build 2 frames sent in parallel on the serial links toward TELL1.

Expected data, if 3 L0_Accept signals are sent respectively on BC0, BC1 and BC2*

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First frame					Second frame					Third frame				
34	1011	1012	301B	301C	34	1011	1012	301B	301C	34	1011	1012	301B	301C
	Channel 1		Channel 0			Channel 1		Channel 0			Channel 1		Channe 2	
Word	MSB			LSB	Word	MSB			LSB	Word	MSB			LS
0	0001	0000	0001	0000	0	0002	0001	0002	0001	0	0003	0002	0003	0002
1	0706	0007	1013	1014	1	1716	0017	1013	1014	1	2726	0027	1013	1014
2	0006	0020	1015	1016	2	0016	0021	1015	1016	2	0026	0022	1015	1016

3	0001	0000	1017	1018	3	1011	0010	1017	1018	3	2021	0020	1017	1018
4	0001	0020	1019	101A	4	0011	0021	1019	101A	4	0021	0022	1019	101A
5	0203	0002	101B	101C	5	1213	0012	101B	101C	5	2223	0022	101B	101C
6	0003	0020	2000	2001	6	0013	0021	2000	2001	6	0023	0022	2000	2001
7	0405	0004	2002	2003	7	1415	0014	2002	2003	7	2425	0024	2002	2003
8	0005	0020	2004	2005	8	0015	0021	2004	2005	8	0025	0022	2004	2005
9	0607	0006	2006	2007	9	1617	0016	2006	2007	9	2627	0026	2006	2007
10	0007	0020	2008	2009	10	0017	0021	2008	2009	10	0027	0022	2008	2009
11	0000	0001	200A	200B	11	0000	0001	200A	200B	11	0000	0001	200A	200B
12	0002	0003	200C	200D	12	0002	0003	200C	200D	12	0002	0003	200C	200D
13	0004	0005	200E	200F	13	0004	0005	200E	200F	13	0004	0005	200E	200F
14	0006	0007	2010	2011	14	0006	0007	2010	2011	14	0006	0007	2010	2011
15	0008	0009	2012	2013	15	0008	0009	2012	2013	15	0008	0009	2012	2013
16	000A	000B	2014	2015	16	000A	000B	2014	2015	16	000A	000B	2014	2015
17	000C	000D	2016	2017	17	000C	000D	2016	2017	17	000C	000D	2016	2017
18	000E	000F	2018	2019	18	000E	000F	2018	2019	18	000E	000F	2018	2019
19	0010	0011	201A	201B	19	0010	0011	201A	201B	19	0010	0011	201A	201B
20	0012	0013	201C	3000	20	0012	0013	201C	3000	20	0012	0013	201C	3000
21	0014	0015	3001	3002	21	0014	0015	3001	3002	21	0014	0015	3001	3002
22	0016	0017	3003	3004	22	0016	0017	3003	3004	22	0016	0017	3003	3004
23	0018	0019	3005	3006	23	0018	0019	3005	3006	23	0018	0019	3005	3006
24	001A	001B	3007	3008	24	001A	001B	3007	3008	24	001A	001B	3007	3008
25	001C	1000	3009	300A	25	001C	1000	3009	300A	25	001C	1000	3009	300A
26	1001	1002	300B	300C	26	1001	1002	300B	300C	26	1001	1002	300B	300C
27	1003	1004	300D	300E	27	1003	1004	300D	300E	27	1003	1004	300D	300E
28	1005	1006	300F	3010	28	1005	1006	300F	3010	28	1005	1006	300F	3010
29	1007	1008	3011	3012	29	1007	1008	3011	3012	29	1007	1008	3011	3012
30	1009	100A	3013	3014	30	1009	100A	3013	3014	30	1009	100A	3013	3014
31	100B	100C	3015	3016	31	100B	100C	3015	3016	31	100B	100C	3015	3016
32	100D	100E	3017	3018	32	100D	100E	3017	3018	32	100D	100E	3017	3018
33	100F	1010	3019	301A	33	100F	1010	3019	301A	33	100F	1010	3019	301A