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L0 Operational Information

Slides used to train RICH shifters to configure the RICH L0 and HPDs

- L0DAQSean.ppt

Recent L0 problems and solutions

- HV effects (especially ramping) often induces upsets in the L0 configuration. The symptoms are typically missing hits on the event display, vertical bars on the event display, FSM transition to ERROR or increase or decrease of column LV current. In some cases it is possible to recover by reconfiguring the affected boards, in other cases it is necessary to cycle the power on the affected boards. This sort of upset usually becomes less frequent once the HV has been stable for some time.

General notes

Please note that correct operation of the L0 boards (configuration, readout etc.) requires the clock signal from the TFC system to be present.

The DNS, Specs and Dim server's are started automatically. These servers run using the Service+ tool on the PCs r1daq01w, r1daq02w for R1 and r2daq02w r2daq01w for R2

Make sure the FSM of the appropriate column in the R2DAQL0 project is in the NOT_READY state (an FSM reset might be necessary), then CONFIGURE. All L0 boards will be in ALICE mode by default at this point.

NOTE: if one of the SPECS masters (which have 4 channels per card) is not working correctly, then the column numbering scheme in the L0 project may differ from that in the LV project, e.g. column C5 is referred to in the L0 project as C1 because the addresses have shifted by 4 (= the number of ports per SPECS master)

Pixel chip test pulses (test rows)

Settings that enabled test rows in the SSB2 on 25/4/7 were (assuming the test flag has been set for some pixels):

- PINT Calibration/test pulse register: 11548451 (i.e. N_start=35, N_stop=55, N_trig=176)
- Pixel chip delay_control DAC: 79
- ODIN Calib. trigger A selected in main panel
- ODIN Calib. trigger delay A set to 205 (and Calib. trigger A window = 3)
- ODIN L0 Latency set to 176

Other settings that were found to work in the SSB2 on 27/4/7 are (all with delay_control=79 and with ODIN L0 latency set to 176):

- N_start=34, N_stop=54, N_trig=176, ODIN Calib. trigger delay A=205, trig. A window=3
- N_start=4, N_stop=24, N_trig=176, ODIN Calib. trigger delay A=175, trig. A window=0
- N_start=5, N_stop=25, N_trig=176, ODIN Calib. trigger delay A=176, trig. A window=0
- N_start=5, N_stop=15, N_trig=176, ODIN Calib. trigger delay A=176, trig. A window=0

Suitable values of TTCrx fine delay 2 were in the range 90-210 (* 104.17ps). Although N_trig settings are given above, it is not known whether the events were correctly labelled as calibration events (the PINT documentation in fact indicates that the N_trig value should be 176-2=174)

On 8th & 9th May, test rows were seen at the pit, with the following settings (different N_start & N_stop values were set on each L0 board):

- Pixel chip DAC 43 ("delay_control") = 79
- PINT N_start = {3...10}, N_stop = {13...20}. N_trig=176
- ODIN Calib. trigger delay A=172, window=0 (calib. trig. A offset should not matter, and worked with values of 128 & 256)
- ODIN L0 latency=176
- ODIN L0 gap length = 1

On 9th May, after another power cycle, the following settings allowed us to see test rows on all HPDs:

- N_{start,stop,trig} = 5,15,176
- Pixel chip delay_control DAC = 79
- ODIN Calib. trigger delay A=170, window=0; ODIN L0 latency = 176; ODIN L0 gap length = 1

On 10th May, with columns 1 and 8 on RICH2 C side, timings that were found to work were:

- N_{start,stop,trig} = 10,20,176
- Pixel chip delay_control DAC = 79
- ODIN Calib. trigger delay A=176 or 175, window=0, ODIN L0 latency=176; ODIN L0 gap length=1

On 10th May, with column 2 on R2C side, timing that was found to work was

- N_{start,stop,trg} = 10,18,176
- PINT_config = 11539466 (=> N_{start,stop,trig)=10,20,176 & ODIN Calib. trig. delay=176 gave some test pulses, but at low efficiency, on R2C col. 2
- PINT_config = > N_{start,stop,trig)=11,21,176 & ODIN Calib. trig. delay=176 gave higher (85-100%) efficiency, on R2C col. 2.

On 26 Aug 2008 R1 test pulses were aligned

- N_{start,stop,trg} = 11,21,176
- PINT_config = 11539723 (=> N_{start,stop,trig)=10,20,176 & ODIN Calib. trig. A delay=176 gave goo efficiency with TTcrx FT2 set to 15700 ps

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This topic: LHCb/RichOperations > RichL0
Topic revision: r5 - 2008-08-26 - SeanBrisbane