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The LHCb Upgrade Silicon Strip Common ASIC - SALT (Silicon ASIC for LHCb Tracking)

People

- Activity conveners: Marek Idzik (AGH-UST UT PI and SALT Project Coordinator), Krzysztof Swientek (SALT Project co-Coordinator), Tomasz Szumlak (LHCb Krakow Upgrade Coordinator)
- Chip designers: Miroslaw Firlej (PLL, DLL), Tomasz Fiutowski (Calibration, I/O, Analog and Chip Integration), Marek Idzik (FE), Jakub Moron (ADC), Krzysztof Swientek (DSP, Digital Implementation) plus other PhD students for various blocks, ...
- Radiation campain coordinator: XXX
- DSP emulation (Tomasz Szumlak)
- Data format specification ( Jianchun Wang)
- Debug testing ( Carlos Abellan Beteta, Jianchun Wang)
- Volume testing ( Olaf Steinkamp)

SALT general description

Silicon strip detectors in the upgraded Tracker of LHCb experiment will use a new 128-channel readout ASIC called SALT. A block diagram of the SALT is shown in figure below. SALT extracts and digitizes analogue signals from the sensor, performs digital processing and transmits a serial output data. It is designed in TSMC CMOS 130 nm technology, and uses a novel architecture comprising an analogue front-end and an ultra-low power (< 0.5 mW) fast (40 MSps) sampling 6-bit ADC in each channel.

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SALT block diagram

Estimated power consumption at 1.2V power supply:

<table>
<thead>
<tr>
<th>Block</th>
<th>Power</th>
<th>N</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog</td>
<td>2.5mW</td>
<td>128</td>
<td>320mW</td>
</tr>
<tr>
<td>Digital</td>
<td>3.16mW</td>
<td>128</td>
<td>405mW</td>
</tr>
<tr>
<td>ASIC</td>
<td>5.66mW</td>
<td>128</td>
<td>725mW</td>
</tr>
</tbody>
</table>
Documents

- Chip specification (VELO, TT and IT): latest version in CDS here
- Overall planning: see VELO, IT, TT planning here
- **SALT User manual**: v3, v4, v5
- External documents: LHCb Upgrade electronics, Electronics Architecture, TFC system-level specs
- AGH SALT development e-logbook web site

SALT tests

- SALT tests

SALT v3 test links

- Tests at Krakow
- Tests at Milano
- Tests at Syracuse

Events

- indico search
- INFN Milano LHCb UT workshop (17-19 May 2016)
- SALT128 submission readiness review (29 February 2016)
- Engineering Design Review of key components of the LHCb Tracker (18-23 June 2015)
- University of Maryland LHCb UT Workshop (7-9 May 2015)
- Workshop on Common ASIC for the LHCb Upgrade (4 July 2012)

Other important events

- UT Bare Stave Production Readiness Review And Electronics Reviews (30 June - 1 July 2016)
- UT Silicon Sensor Type-A Pre-production Readiness Review (17 June 2016)
- Engineering Design Review for the Detector Box of the LHCb Upstream Tracker (13 June 2016)
- UT Electronics Review (20-21 October 2014)
- UT Conceptual Design Review (14-15 November 2013)

SALT Publications and Conferences

- K. Swientek (on behalf of UT LHCb collaboration), SALT ASIC for LHCb tracking, Front End Electronics 2016, Krakow, Poland

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