Table of Contents

Table of Contents

JINF-T specific code description (version R04/20100803)

1. Introduction

The JINFT will have to manage the tracker slow control devices using a similar procedure as the one implemented in the JINF-E and JINF-R (1).

The JINFT can control through the LeCroy bus the four TPSFE, and the two TBS of the T-Crate, but also the S9011AT board of the TPD. In a similar way as for the JINFE or JINFU, specific parameters have been implemented into the JINFT to control those devices. Following table lists the parameters as well as the corresponding device:

Name	***Location***	***Parameter group in JINFT***	***Words used***	***Relative start address***	
S9011AT	Tracker Power Distribution	2	48	0	
TPSFE 4	Slot 4 of T-Crate	3	92	48	(0x30)
TPSFE 6	Slot 6 of T-Crate	4	92	140	(0x8C)
TPSFE 14	Slot 14 of T-Crate	5	92	232	(0xE8)
TPSFE 16	Slot 16 of T-Crate	6	92	324	(0x144)
TBS 5	Slot 5 of T-Crate	7	58	416	(0x1A0)
TBS 15	Slot 15 of T-Crate	8	58	474	(0x1DA)
FPGA control		9	2	532	(0x214)

The total sub-detector parameter space in the JINFT is thus 534 words large, and 267 parameters are defined.

Next sections describe the list of parameters implemented into JINFT.

2.

S9011AT is the communication and control board of the Tracker Power Distribution. It is equipped with two FPGAs. In normal operations only one should be powered, even if both can be operated at the same time. In that case, both FPGA commands are ORed. Here are the parameters implemented in the JINF-T code:

S9051 control:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
2	1	0	S9051_0 S control	1	0, 1	2
2	1	1	S9051_0 K control	1	0, 1	4
2	1	2	S9051_1 S control	1	0, 1	6
2	1	3	S9051_1 K control	1	0, 1	8
2	1	4	S9051_2 S control	1	0, 1	10
2	1	5	S9051_2 K control	1	0, 1	12
2	1	6	S9051_3 S control	1	0, 1	14
2	1	7	S9051_3 K control	1	0, 1	16

S9053 control:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
2	2	0	S9053_0 Hot control	1	0, 1	18
2	2	1	S9053_0 Cold control	0	0, 1	20
2	2	2	S9053_1 Hot control	1	0, 1	22
2	2	3	S9053_1 Cold control	0	0, 1	24

S9055 control:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
2	3	0	S9055_0 Hot control	1	0, 1	26
2	3	1	S9055_0 Cold control	0	0, 1	28
2	3	2	S9055_1 Hot control	1	0, 1	30
2	3	3	S9055_1 Cold control	0	0, 1	32

2.1 Register contents and error codes

The S9011AT has five registers in which the real data are stored. The original data are stored in the following parameters. Of particular interest is the trip register, which indicates over-current events for the DC-DC converters.

Group	*SubG*	*ID*	*Description*	*Relative address*
2	4	0	Error word	34

2	4	1	Over-current word	36
2	4	2	Trip bits (content of S9011AT register 4)	38
2	5	0	Content of S9011AT register 0	40
2	5	1	Content of S9011AT register 1	42
2	5	2	Content of S9011AT register 2	44
2	5	3	Content of S9011AT register 3	46

An error word is located at relative address 34, its bit description is as follows:

Bit	***Description***
0	Error reading register 0
1	Error reading register 1
2	Error reading register 2
3	Error reading register 3
4	Error reading register 4
13	Actel brother trip
15	Actel power on bit

The over-current word, at relative address 36, indicates if a specific DC-DC converter has been switched off due to an over-current situation. Its bit description is the same as for the trip register (relative address 38):

Bit	***Description***
0	S9051_0 S
1	S9051_0 K
2	S9051_1 S
3	S9051_1 K
4	S9051_2 S
5	S9051_2 K
6	S9051_3 S
7	S9051_3 K
8	S9053_0 Hot
9	S9053_0 Cold
10	S9053_1 Hot
11	S9053_1 Cold
12	S9055_0 Hot
13	S9055_0 Cold
14	S9055_1 Hot
15	S9055_1 Cold

3 The TPSFE

The Tracker Power Supply for the Front End electronics controls six ladders. There is one TPSFE for each poser group. It is equipped with two FPGAs. In normal operations only one should be powered, even if both can be operated at the same time. In that case, both FPGA commands are ORed. The parameters implemented in the JINF-T are the following:

TDR controls:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
3, 4, 5, 6	1	0	TDR 0 control	1	0, 1	2
3, 4, 5, 6	1	1	TDR 1 control	1	0, 1	4
3, 4, 5, 6	1	2	TDR 2 control	1	0, 1	6
3, 4, 5, 6	1	3	TDR 3 control	1	0, 1	8
3, 4, 5, 6	1	4	TDR 4 control	1	0, 1	10
3, 4, 5, 6	1	5	TDR 5 control	1	0, 1	12
3, 4, 5, 6	1	6	TDR auto-off mode	1	0, 1	14

S-side linear regulator controls:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
3, 4, 5, 6	2	0	LRS 0 control	1	0, 1	16
3, 4, 5, 6	2	1	LRS 1 control	1	0, 1	18
3, 4, 5, 6	2	2	LRS 2 control	1	0, 1	20
3, 4, 5, 6	2	3	LRS 3 control	1	0, 1	22
3, 4, 5, 6	2	4	LRS 4 control	1	0, 1	24
3, 4, 5, 6	2	5	LRS 5 control	1	0, 1	26
3, 4, 5, 6	2	6	LRS auto-off mode	1	0, 1	28

K-side linear regulator controls:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
3, 4, 5, 6	3	0	LRK 0 control	1	0, 1	30
3, 4, 5, 6	3	1	LRK 1 control	1	0, 1	32
3, 4, 5, 6	3	2	LRK 2 control	1	0, 1	34
3, 4, 5, 6	3	3	LRK 3 control	1	0, 1	36
3, 4, 5, 6	3	4	LRK 4 control	1	0, 1	38
3, 4, 5, 6	3	5	LRK 5 control	1	0, 1	40
3, 4, 5, 6	3	6	LRK auto-off mode	1	0, 1	42

3.1 Register contents and error code

The TPSFE information is actually stored in 9 registers. The content of those registers are interpreted by the JINF-T to give an easier (human understandable) information stored in the READ parameters described in

the previous section. Nevertheless, the original information is also stored into the JINF-T memory, as well as the trip counters, interesting information in case of power supply troubles. Next table describes those data.

Group	*SubG*	*ID*	*Description*	*Relative address*
3, 4, 5, 6	4	0	Error word	44
3, 4, 5, 6	5	0	TDR 0 digital power supply trip counter	46
3, 4, 5, 6	5	1	TDR 1 digital power supply trip counter	48
3, 4, 5, 6	5	2	TDR 2 digital power supply trip counter	50
3, 4, 5, 6	5	3	TDR 3 digital power supply trip counter	52
3, 4, 5, 6	5	4	TDR 4 digital power supply trip counter	54
3, 4, 5, 6	5	5	TDR 5 digital power supply trip counter	56
3, 4, 5, 6	6	0	LRS 0 trip counter	58
3, 4, 5, 6	6	1	LRS 1 trip counter	60
3, 4, 5, 6	6	2	LRS 2 trip counter	62
3, 4, 5, 6	6	3	LRS 3 trip counter	64
3, 4, 5, 6	6	4	LRS 4 trip counter	66
3, 4, 5, 6	6	5	LRS 5 trip counter	68
3, 4, 5, 6	7	0	LRK 0 trip counter	70
3, 4, 5, 6	7	1	LRK 1 trip counter	72
3, 4, 5, 6	7	2	LRK 2 trip counter	74
3, 4, 5, 6	7	3	LRK 3 trip counter	76
3, 4, 5, 6	7	4	LRK 4 trip counter	78
3, 4, 5, 6	7	5	LRK 5 trip counter	80
3, 4, 5, 6	8	0	Actel brother trip counter	82
3, 4, 5, 6	9	0	Content of TPSFE register 0	84
3, 4, 5, 6	9	1	Content of TPSFE register 1	86
3, 4, 5, 6	9	2	Content of TPSFE register 2	88
3, 4, 5, 6	9	3	Content of TPSFE register 3	90

Finally, an error code is found at relative address 44, and is parameter 0 of sub-group 4. Its bit description is the following:

Bit	*Description*
0	Error reading register 0
1	Error reading register 1
2	Error reading register 2
3	Error reading register 3
4	Error reading register 4
5	Error reading register 5
6	Error reading register 6
7	Error reading register 7
8	Error reading register 8
15	Actel power on

4. TBS

The Tracker Bias Supply provides the voltages for 12 ladders. This board has rather few controls, but provides many voltage and current measurements. The TBS is equipped with two FPGAs. In normal operations only one should be powered, even if both can be operated at the same time. In that case, both FPGA commands are ORed.

The parameters implemented in the JINF-T are the following:

Bias voltage controls:

In the following table, 0 corresponds to the off status, 1 corresponds to the on status.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*	*Relative address*
7, 8	1	0	LR 0 Hot control	1	0, 1	2
7, 8	1	1	LR 0 Cold control	1	0, 1	4
7, 8	1	2	LR 1 Hot control	1	0, 1	6
7, 8	1	3	LR 1 Cold control	1	0, 1	8
7, 8	1	4	LR 0 Hot 80V mode	1	0, 1	10
7, 8	1	5	LR 0 Cold 80V mode	1	0, 1	12
7, 8	1	6	LR 1 Hot 80V mode	1	0, 1	14
7, 8	1	7	LR 1 Cold 80V mode	1	0, 1	16

NOTES:

1. The linear regulator internal circuit design is done in such a way that when the HOT part is active, the COLD part is necessarily off. If the bias voltage produced by the LR HOT goes under a given threshold, the COLD part is automatically activated. But for this to happen, all LR have to be explicitly ON.
2. The 80V mode is the standard linear regulator voltage. It can be reduced to 60V setting the corresponding variable to 0.

4.1 Register contents

The TBS information is actually stored in 18 registers. The contents of those registers are interpreted by the JINF-T to give an easier (human understandable) information stored in the READ parameters described in the previous section. Nevertheless, the original information is also stored into the JINF-T memory, as well as the ADC values corresponding to voltages and currents. Next table describes those data.

Group	*SubG*	*ID*	*Description*	*Relative address*
7, 8	2	0	Error word 0	18
7, 8	2	1	Error word 1	20
7, 8	3	0	Content of TBS register 0	22
7, 8	3	1	Content of TBS register 1	24
7, 8	4	0	Voltage of LR0 Hot	26
7, 8	4	1	Voltage of LR0 Cold	28
7, 8	4	2	Voltage of LR1 Hot	30
7, 8	4	3	Voltage of LR1 Cold	32
7, 8	5	0	Current of channel 0	34
7, 8	5	1	Current of channel 1	36
7, 8	5	2	Current of channel 2	38

7, 8	5	3	Current of channel 3	40
7, 8	5	4	Current of channel 4	42
7, 8	5	5	Current of channel 5	44
7, 8	5	6	Current of channel 6	46
7, 8	5	7	Current of channel 7	48
7, 8	5	8	Current of channel 8	50
7, 8	5	9	Current of channel 9	52
7, 8	5	10	Current of channel 10	54
7, 8	5	11	Current of channel 11	56

Two error words are located at relative addresses 18 and 20.

Description of first error word is as follows:

Bit	***Description***
0	Error reading register 0
1	Error reading register 1
8	LR0 Hot status (*1=off*)
9	LR1 Hot status (*1=off*)
13	Actel brother trip
15	Actel powered on

The bit description of the second error word is the following:

Bit	***Description***
0	Error reading register 16
1	Error reading register 17
2	Error reading register 18
3	Error reading register 19
4	Error reading register 20
5	Error reading register 21
6	Error reading register 22
7	Error reading register 23
8	Error reading register 24
9	Error reading register 25
10	Error reading register 26
11	Error reading register 27
12	Error reading register 28
13	Error reading register 29
14	Error reading register 30
15	Error reading register 31

5. Crate status parameters

A ninth parameter group is used to describe the crate status. Only one parameter is used, the actel mask word which describes which FPGA of each board must be used. In addition, for the S9011AT, this mask describes which communication cable should be used.

Group	*SubG*	*ID*	*Parameter*	*Default value*	*Possible values*
9	0	0	Actel mask	0x5551	0 to 0xFFFF

The actel mask word is described in the following table:

Bit	*Description*	*Default value*
0	S9011AT actel A, connector 0	1
1	S9011AT actel B, connector 0	0
2	S9011AT actel A, connector 1	0
3	S9011AT actel B, connector 1	0
4	TPSFE 4 actel A	1
5	TPSFE 4 actel B	0
6	TPSFE 6 actel A	1
7	TPSFE 6 actel B	0
8	TPSFE 14 actel A	1
9	TPSFE 14 actel B	0
10	TPSFE 16 actel A	1
11	TPSFE 16 actel B	0
12	TBS 5 actel A	1
13	TBS 5 actel B	0
14	TBS 15 actel A	1
15	TBS 15 actel B	0

If the bit value is set to 1, the corresponding actel (and connector if applicable) will be used for the slow control operations. During initialization, according to the bit values, the corresponding actel will be switched on (for a bit set to 1) or off (bit set to 0).

See appendix B for more details on the actel mask.

6. JINF SDPROC_WR command

The SDPROC_WR command is used to execute most of the commands described here. A general framework has been implemented into the mainframe, nevertheless it has not yet been documented. Thus we give here a tentative documentation.

The command sSDPROC_WR corresponds to AMSWIRE command 54. It accepts the following parameters.

- 0x1001 for the JINF-T (no other parameter needed). sEVBLD_INIT is called. This subroutine itself calls sSDCONFIG_DEFAULT_LB , then, calls sSDCONFIG_INIT_LB . Parameters are reset to their values, and the applied to the slow control deviced.
- 0x1002 for the JINF-T. Another parameter, the crate mask (stored in cDM_CRATE_MASK) is needed. For the crate mask parameter, the bit description is the following:
    - bit 15: call sSDCONFIG_INIT_DM (parameter group 0 initialization: slave masks);
    - bit 14: call sSDCONFIG_INIT_IO (parameter group 1 initialization: SSF, BUSY mask, trigger to hold time). After this, and in any case, sSDCONFIG_INIT_LB is called.
      Any other parameter triggers a call to sSDPROC_WR_LB :

- 0x1003 triggers the execution of sSDCONFIG_INIT_LB only.
- 0x1004 triggers the execution of sSDCONFIG_DEFAULT_LB only.
- 0x1005 takes the beforehand readout status and makes them the default ones.
- 0x1100 switches off all the analogical power supplies.
- 0x1110 with an additional parameter (0 or 1) disables or enables the S9053 command controls.
- 0x1111 with an additional parameter (0 or 1) disables or enables the TPSFE auto-off command controls.
- 0x1200 with an additional parameter (0 or 1) executes S9053_x Hot to Cold transition (to be executed by JINF-T A when parameter is 1, and JINF-T B when parameter is 0).
- 0x1201 Switches on S9011 actel brother, and writes S9011 parameters to both Actels.
- 0x1202 Switches off one of the two S9011 Actels according to a mask defined by the execution of parameter 0x1201.

6.1 0x1003: Power supplies settings update

Parameter 0x1003 triggers the application of all the power supply settings. Typical uses are:

- Application of the default settings after power-on.
- Application of new settings after having modified the parameters in the Jinf-T memory. E.g. if you wish to activate S9055_0 cold instead of S9055_0 hot, you would perform the following sequence:
    1. 2E49 1001 2301 1 // switch on S9055_0 cold
    2. 2E54 1003 // apply the new setting: now S9055_0 cold is on
    3. 2E49 1001 2300 0 // switch off S9055_0 hot
    4. 2E54 1003 // apply the new setting: now S9055_0 hot is off
- The S9053 control is protected and settings are only applied if they have been previously enabled, as shown in the following sequence:
    1. 2E49 1001 2202 0 // switch off S9053_1 hot
    2. 2E54 1200 1 // allows settings to be applied also to S9053 DC-DC converters
    3. 2E54 1003 // apply the settings... are you sure of what you are doing ?
    4. 2E54 1200 0 // disables the S9053 control

6.2 0x1004: Reset parameters to default

This parameter allows to reset all the power supply parameters to their default values, defined in the DSP code itself. Once the parameters are reset to default, you still need to apply them:

1. 2E54 1004 // reset the parameters to their factory settings .
2. 2E54 1003 // apply the settings to the power supplies

6.3 0x1005: Takes previously status readout as default settings

This command is particularly useful for the S9053 Hot to Cold transition. It allows the JINF-T, after having examined the actual status of the power supplies, to save into the memory the present state as the default state. A typical sequence follows:

1. 2E14 1001 // get the present power supplies status
2. 2E54 1005 // make present status default

To reset the parameters to their factory settings , see section 6.2 .

6.4 0x1100: Analog voltages switch-off

Switches off all S9051 and S9055 DC-DC converters.

6.5 0x1110: S9053 control enable

This command needs a second parameter: 0 or 1. For an example, see section 6.1 .

6.6 0x1111: TPSFE auto-off control enable

Every time the auto-off setting is written in the ACTEL register, the corresponding trip counter is reset to 0. This behavior might be not convenient. This is why in the JINF-T the auto-off control setting is disabled. Here is a typical sequence:

1. 2E54 1111 1 // enables auto-off control
2. 2E54 1003 // apply settings, in particular, all trip counters will be reset to 0.
3. 2E54 1111 0 // disables auto-off control

6.7 0x1200: S9053 hot to cold transition

An additional parameter is needed: 0 for S9053_0 and 1 for S9053_1 . This command must be used with care, keep in mind that to obtain the expected result:

- 2E54 1200 0 must be executed by JINF-T ***B*** and S9011 Actel ***Cold*** .
- 2E54 1200 1 must be executed by JINF-T ***A*** and S9011 Actel ***Hot*** .

6.8 0x1201: S9011 Actel brother switch-on and copy of settings

This command is a necessary step to perform a complete S9053 Hot to Cold transition. When an Actel is switched on, it provides the factory settings to S9011. During an Actel to Actel brother transition is it thus necessary to transfer the non-factory settings to the newly switched-on Actel. This 1201 command executes the following steps:

1. Switch on Actel brother.

2. Applies the power supply parameters to both Actels.

For an application example, see section 9.

6.9 0x1202: S9011 Actel exchange

Still being part of the S9053 Hot to Cold procedure, this command is the successive step of command 0x1201.

For an application example, see section 9.

7. JINF SDPROC_RD command

The SDPROC_RD command is used to execute most of the commands described here. A general framework has been implemented into the mainframe, nevertheless it has not yet been documented. Thus we give here a tentative documentation.

The command sSDPROC_RD corresponds to AMSWIRE command 14. It accepts the following parameters.

- 0x1001 the JINF-T (no other parameter needed). The subroutines sSDCONFIG_VERIFY_DM , sSDCONFIG_VERIFY_IO , sSDCONFIG_VERIFY_LB are executed. In output, the JINF first gives the content of DM(cDM_CRATE_STATUS) , then the error code for group 0 and the error code for group 1.
  The purpose of the sSDCONFIG_VERIFY_XX subroutines is the following:
  1. Refresh in the parameter memory the active parameter values.
  2. Count the number of discrepancies between wished settings and actual setting: if there are no discrepancies, the corresponding bit cCRATE_CDDC_XX_MASK_BIT of is set to 1. The error code on the other hand contains the number of discrepancies. Then sSDPROC_RD_LB_STATUS_SHORT, is called: first, the number of LeCroy readout errors is given, then, the list of discrepancies is given, with the following format:
     1. Parameter number (included group and subgroup IDs);
     2. Readout value.
- 0x1002 for the JINFT, no other parameter is needed. Also here the subroutines sSDCONFIG_VERIFY_DM , sSDCONFIG_VERIFY_IO , sSDCONFIG_VERIFY_LB are executed. Once those subroutines have been executed, the whole parameter list (expected and really acquired) is sent in output.
- 0x1011: provides the list of parameters with actual settings (use first a 0x1001).
- 0x1012: provides the TBS ADC values (use first a 0x1001).
- 0x1110: indicates the status of S9053 control (see previous section).
- 0x1111: indicates the status of TPSFE auto-off control (see previous section).

7.1 0x1011: Get list of actual settings

Using this parameter, you will get the power supply states stored in the JINF-T memory. This means that you first need to call a 0x1001 or 0x1002 procedure to update the JINF-T memory. Here a is sequence example:

1. 2E14 1001 // update the power supply states, store them in memory, and provide list of discrepancies
2. 2E14 1011 // get whole list of actual settings

The data provided by the JINF-T are pairs of values: parameter name, followed by its content. Note that this values is NOT the setting you decided to apply to the power supply, but the *actual* state as seen by the JINF-T.

The output format is described in the following table:

Word #	***Content***
0	Actual Actel mask
1	Number of discrepancies
2	0x2100 (parameter name)
3	Actual value corresponding to setting 0x2100
4	0x2101 (parameter name)
5	Actual value corresponding to setting 0x2101
...	...

408	0x9000 (parameter name)
409	Actual value corresponding to setting 0x9000

7.2 0x1012: Get list of TBS ADC values

With this parameter you get the list of both TBS ADC values. You need first to update the JINF-T memory with the actual values, as shown in the following sequence:

1. 2E14 1001 // update the power supply states, store them in memory, and provide list of discrepancies
2. 2E14 1012 // get the TBS ADC values.

The output format is as follows:

Word #	***Content***
0	Error word 1 of TBS 5
1	Voltage of LR0 Hot, TBS 5
2	Voltage of LR0 Cold, TBS 5
3	Voltage of LR1 Hot, TBS 5
4	Voltage of LR1 Cold, TBS 5
5	Current of channel 0, TBS 5
...	...
16	Current of channel 11, TBS 5
17	Error word 1 of TBS 15
18	Voltage of LR0 Hot, TBS 15
...	...
33	Current of channel 11, TBS 5

8. Configuration file management

The JINFT default configuration parameters can be altered by a configuration file. The configuration file principles are described elsewhere (2). Here we only want to insist on some important aspects:

- The configuration file is loaded with the 2E46 command, but if it has the default flag (set through the 2E48 command), it is automatically loaded at JINFT program initialization.
- When the configuration file is loaded through the 2E46 command, the parameters are modified according to the file contents. ***But for the new settings to applied, the user still needs to send the 2E54 1003 command*** , even if it has the default file flag.
- During the initialization process, a default configuration file is loaded, if it exists. In such a case, all the parameters are executed (like if a 2E54 1003 would be automatically called). Please note that even if the configuration file does not alter groups 2 to 9, those parameters are anyway applied.
- ***Thus it is mandatory that at maximum only one JINF has a default parameter file, typically JINF-A.***

9. S9053 Hot to Cold transitions

While they remain implemented in the Jinf-T it has been decided not to use the macro-functions described here, but instead to send direct LeCroy commands to the Jinf at power-on time.

The S9053 power supply particular case is described in another document (3). Here is the command sequence to execute safely a S9053 hot to cold transition. The default S9011AT Actel Hot selection (for simplicity it is the same setting for both JINFT A and B) determines the kind of sequence to follow. But this decision explains the various number of operations to apply depending on the final configuration to obtain.

9.1 S9053_0 and S9053_1 hot to cold

This operation sequence must be executed only after a general switch on.

Jinf	*Command*	*Comment*	*Time (s)*
A	2E54 1003	Sets the default operation settings	1.10
A	2E54 1200 1	Hot to Cold transition of S9053_1	1.83
A	2E54 1201	Activates S9011 Actel Cold and applies the actual settings to both Actels.	0.73
A	2E54 1202	Switches off the S9011 Actel Hot	1.09
B	2E14 1001	Jinf B gets the actual settings of the power supplies	0.01
B	2E54 1005	Jinf B takes as default the actual settings	0.00
B	2E54 1200 0	Hot to Cold transition of S9053_0	1.83
A	2E14 1001	Jinf A gets the actual settings of the power supplies	0.01
A	2E54 1005	Jinf A takes as default the actual settings	0.00
A	2E54 1201	Activates S9011 Actel Hot and applies the actual settings to both Actels.	0.73
A	2E54 1202	Switches off S9011 Actel Cold.	1.09
A	2E54 1005	Jinf A takes as default the actual settings	0.00
			8.42

After this sequence, the S9053_0 Cold and S9053_1 Cold are active, as well as Actel Hot of S9011.

9.2 Only S9053_1 hot to cold transition

This operation sequence must be executed only after a general switch on.

Jinf	*Command*	*Comment*	*Time (s)*
A	2E54 1003	Sets the default operation settings	1.10
A	2E54 1200 1	Hot to Cold transition of S9053_1	1.83
			2.93

At the end of this sequence, S9053_1 Cold is activated, and Actel Hot of S9011AT is active.

9.3 Only S9053_0 hot to cold transition

This operation sequence must be executed only after a general switch on.

Jinf	*Command*	*Comment*	*Time (s)*
B	2E54 1003	Sets the default operation settings	1.10
B	2E54 1201	Activates S9011 Actel Cold and applies the actual settings to both Actels.	0.73
B	2E54 1202	Switches off S9011 Actel Hot	1.09
B	2E54 1200 0	Hot to Cold transition of S9053_0	1.83
B	2E54 1201	Activates S9011 Actel Hot and applies the actual settings to both Actels.	0.73

B	2E54 1202	Switches off S9011 Actel Cold.	1.09
			6.57

At the end of this sequence, S9053_0 Cold is activated, and Actel Hot of S9011AT is active.

9.4 JINF failures

The previous operations need the use of both JINFT A and B. If only one JINF remains available, a fully secure transition is not possible anymore: the remaining JINF will have to execute the transition for the S9053 which is powering himself. At that point, the simplest is to implement the settings directly in the default configuration file:

Parameter	*For JINFT A*	*For JINFT B*
2200	0	1
2201	1	0
2202	1	0
2203	0	1
9000	5552	5551

9.4.1 Operation sequence for JINFT A

The default configuration file activates the S9011AT Actel Cold. The JINF A contains the new S9053_0 settings, but are not applied yet, as the S9053 settings need to be explicitly enabled:

1. Enable the S9053 operations: 2E54 1110 1
2. Apply the power supply settings: 2E54 1003
3. Boot and reload the JINF program: a glitch on 3.3 V volts has happened, the JINF state is unknown.
4. Activate the Actel Hot: 2E54 1201
5. Switch off the Actel Cold: 2E54 1202
6. Execute the S9053_1 hot to cold transition, as described in section 9.2

9.4.2 Operation sequence for JINFT B

The default configuration file contains the new S9053_1 settings, but they are not applied yet, as the S9053 settings need to be explicitly enabled:

1. Enable the S9053 operations: 2E54 1110 1
2. Apply the power supply settings: 2E54 1003
3. Boot and reload the JINF program: a glitch on 3.3 V volts has happened, the JINF state is unknown.
4. Execute the S9053_0 hot to cold transition, as described in section 9.3

9.5 S9011 Actel failures

In case of Actel failure, a clean transition is for the S9053 powering the remaining Actel is not possible. It is even not possible to perform a glitch, as the Actel is anyway reset to its default settings, i.e. S9053_x Hot active.

The only one solution is to have for a very short time both S9053 Hot and Cold on, enabling the Actel to be constantly powered. Is this solution acceptable ? I do not think so...

9.6 JINF and Actel failures

See section 9.5 .

APPENDIX A: Device buses and addresses

The devices are addressed by means of a bus number and a geographic address. In the case of the Tracker crate, more than one board is connected to a same bus. The following table lists the various devices, their corresponding bus address and geographic address.

Board / Actel / connector	***Bus***	***Address***
S9011AT actel A, connector 0	0x40	3
S9011AT actel B, connector 0	0x50	
S9011AT actel A, connector 1	0x60	
S9011AT actel B, connector 1	0x70	
TPSFE 4 actel A	0x00	4
TPSFE 4 actel B	0x20	
TPSFE 6 actel A	0x00	6
TPSFE 6 actel B	0x20	
TPSFE 14 actel A	0x10	14 = 0x0E
TPSFE 14 actel B	0x30	
TPSFE 16 actel A	0x10	16 = 0x10
TPSFE 16 actel B	0x30	
TBS 5 actel A	0x00	5
TBS 5 actel B	0x20	
TBS 15 actel A	0x10	15 = 0x0F
TBS 15 actel B	0x30	

NOTES:

1. For the Actels, the denominations A and B are often replaced by Hot and Cold .
2. Connector 0 of S9011AT provides the 3.3 V from S9053_0 while connector 1 provides the 3.3V from S9053_1. Actel A of S9011AT is powered from connector 0, while Actel B is powered from connector 1. Pay attention to any 3.3V manipulations...

APPENDIX B: Actel masks

The actel mask is used to decide which FPGA (and in the case of the S9011AT, which connector) to use to communicate with the power supply device.

The mask must comply with some rules:

1. At least one FPGA must be on.
2. It is preferred to have only one FPGA on.
3. For the S9011AT, only one line at a time should be used (for simplicity).

Thus the procedure followed by the JINF-T is the following:

1. Switch on the FPGAs according to the mask description (call sACTEL_SETON);
2. Test which FPGAs are really on, and store the results into memory (call sACTEL_CHECK_ON);
3. Apply the slow-control settings to all active FPGAs;
4. Switch off the FPGAs according to the mask description (call sACTEL_SETOFF);
5. Test which FPGAs are really on, and store the results into memory (call sACTEL_CHECK_ON).

The mask result will be of the same format as the one described in section 5.

APPENDIX C: Initialization procedures

The default factory settings programmed into the Actels are close the those necessary for a normal tracker operation. Thus the simplest way to proceed to an initialization is to execute a power cycle on every Actel. This solution, though simple is not indicated for a three-year operation time, considering that a total initialization is foreseen every 30 minutes.

This is why the standard initialization procedure will be to explicitly write into the FPGA registers the correct operation settings. This is executed by the following commands:

- TPSFE: call sTPSFE_INIT
- TBS: call sTBS_INIT
- S9011AT: call sS9011_INIT

In the initialization phase, the Actel Brother control are not altered, as it is done through the Actel mask control.

APPENDIX D: JINFT subroutine descriptions

D.1 sSDCONFIG_DEFAULT_LB

This subroutine defines the default parameters for the different JINFT groups 2 to 9. The following subroutines are called:

- sSDCONFIG_DEFAULTS_S9011
- sSDCONFIG DEFAULTS_TPSFE
- sSDCONFIG_DEFAULTS_TBS
- sSDCONFIG_DEFAULTS_TCRATE

The default parameters ask the S9055 cold DC-DC converters to be off, as well as the FPGA cold to be off. A special case regards the S9053 hot and cold configuration, for which an only cold configuration should be desirable.

Note that also the Actel register contents are set to the corresponding expected value.

The memory spaces reserved for the readout values are initialized to the arbitrary value 0xBAC0. This is useful in case of debugging operations, to know if the Jinf operated a successful LeCroy reading and storing into memory.

D.2 sCDDC_LB_COMMAND

Sends the LeCroy command, after having added, if necessary, the parity bit on the W0 word.

D.3 sCDDC_LB_COMMAND_INIT

Initializes the LeCroy bus.

D.4 sACTEL_LB_TEST

This command tests if an FPGA replies to a standard read command. If it does not, it is considered that is it not powered. Reply: AR = 0 means ok, AR = 1 means not ok.

D.5 sACTEL_LB_ON

Sends to FPGA register 0 the content of AR. Depending on the content, switches on or off the brother FPGA.

D.6 sACTEL_SETON

This subroutine switches on the FPGAs (hot or cold) of the various devices, according to the predefined mask located in DM(cDM_CDDC_LB_OFFSET + cDM_CDDC_LB_ADDR_TCRATE) .

D.7 sACTEL_SETOFF

This subroutine switches off the FPGAs (hot or cold) of the various devices, according to the predefined mask locate in DM(cDM_CDDC_LB_OFFSET + cDM_CDDC_LB_ADDR_TCRATE) .

D.8 sACTEL_CHECK_ON

The subroutine checks every FPGA to see if it is on, and builds a corresponding mask at DM(cDM_CDDC_LB_OFFSET + cDM_CDDC_LB_ADDR_TCRATE + 1) .

D.9 sSDCONFIG_INIT_LB

This subroutine performs the following operations:

1. Initialization of the LeCroy buses;
2. Switches on the FPGAs according to the desired mask (sACTEL_SETON)
3. Switches off the FPGAs according to the desired mask (sACTEL_SETOFF).
4. The mask of the FPGAs actually present is done (sACTEL_CHECK_ON).
5. The configuration parameters are then applied, communicating with the FPGAs identified at point 4. It is important to note that nothing prevents the subroutine from setting both hot and cold FPGAs of a same device (and even the line choice for the S9011AT). This flexibility is intentional.

Subroutines called: sTPSFE_INIT, sTBS_INIT, sS9011_INIT.

D.10 sTPSFE_INIT

Sets the TPSFE registers according to the parameters of groups 3 to 6. An exception is register 0, which controls the brother FPGA: it is for now not set, as this action is redundant with sACTEL_SETON and sACTEL_SETOFF.

D.11 sTBS_INIT

Sets the TBS registers according to the parameters of groups 7 and 8. An exception is register 0, which controls the brother FPGA: it is for now not set, as this action is redundant with sACTEL_SETON and sACTEL_SETOFF.

D.12 sS9011_INIT

Sets the S9011AT registers according to the parameters of group 2. An exception is register 0, which controls the brother FPGA: it is for now not set, as this action is redundant with sACTEL_SETON and sACTEL_SETOFF.

D.13 sSDCONFIG_VERIFY_LB

This subroutine executes the following procedures:

1. Initializes all the LeCroy buses.
2. Checks which FPGA is active, using sACTEL_CHECK_ON.
3. For each device, reads out the registers content. If both FPGAs of a same device are powered, they will be both readout. On the other hand, only the results of the last readout FPGA will be kept (i.e. the COLD one).
4. Once all parameters are readout, they are compared with those initially set in the JINFT memory.
5. If the number of discrepancies is non-zero bit cCRATE_CDDC_LB_MASK_BIT (=13) of DM(cDM_CRATE_STATUS) is set to 1.

Calls sTPSFE_VERIFY, sTBS_VERIFY, sS9011_VERIFY, sSDCONFIG_CHECK_PARAMS.

Is called by: sSDPROC_RD and sEBVLD_INFO.

D.14 sSDCONFIG_CHECK_PARAMS

This subroutine simply counts the discrepancies between two sets of data. The starting address is given by I0, and the number of parameters to test is given by AR. The number of discrepancies is added to AF.

D.15 sTPSFE_VERIFY

This subroutine reads out the TPSFE registers, interprets their content, and fills the JINFT memory with those readout parameters. Builds the error word as described in section 2.1 . If there is a readout failure, the JINFT corresponding register content is filled with the 0xDEAD value.

Calls sCDDC_LB_READ_COMMAND, sSDCONFIG_SET_ERROR.

D.16 sCDDC_LB_READ_COMMAND

Sends a LeCroy read command. In particular takes into account the register address, for which a special bit manipulation is necessary if the register address is greater than 7. Moreover, once the reading is executed, a control is done on bit 15 of word R0, if the test fails (i.e. there is a read error), AR is non-zero.

D.17 sSDCONFIG_SET_ERROR

Performs AF OR MR0, where AF contains the error value to add to the initial error word stored in MR0.

D.18 sTBS_VERIFY

This subroutine reads out the TBS registers, interprets their content, and fills the JINFT memory with those readout parameters. Builds two error words as described in section 3.1 . If there is a readout failure, the corresponding JINFT register content is filled with 0xDEAD value.

Calls sCDDC_LB_READ_COMMAND, sSDCONFIG_SET_ERROR, sTBS_SET_ERROR.

D.19 sTBS_SET_ERROR

Particular subroutine for the TBS readout errors when registers are >15 (voltage and current registers). In case of error, sets to 1 the bit corresponding to the register with failure. Moreover, the 0xDEAD value is stored.

D.20 sS9011_VERIFY

This subroutine reads out the S9011AT registers, interprets their content, and fills the JINFT memory with those readout parameters. Builds two error words, as described in section 1.1 . If there is a readout failure, the corresponding JINFT register content is filled with 0xDEAD value.

Calls sCDDC_LB_READ_COMMAND, sSDCONFIG_SET_ERROR.

D.21 sSDCONFIG_WR_LB

Sets the parameter value according to its group, subgroup and id.

The subroutine is called by sSDCONFIG_WR (from amswire command 49).

Calls sSDCONFIG_WR_LB_SET_PARAMETER and sSDCONFIG_WR_LB_SET_TBS_PARAMETER.

D.22 sSDCONFIG_WR_LB_SET_PARAMETER

Writes into the memory the configuration parameter. Applies a mask to only write 0 or 1.

Called by sSDCONFIG_WR_LB.

D.23 sSDCONFIG_WR_LB_SET_TBS_PARAMETER

Checks if parameter id corresponds to a voltage setting or a voltage control. For voltage control, applies a mask to write only 0 or 1, for a voltage setting, checks if the parameter is 60, else it is set to 80.

Called by sSDCONFIG_WR_LB.

D.24 sSDCONFIG_RD_LB

Reads the content of one parameter (as it has been written by sSDCONFIG_WR_LB).

Is called by sSDCONFIG_RD (amswire command 9).

Calls sSDCONFIG_RD_LB_GET_PARAMETER.

D.25 sSDCONFIG_RD_LB_GET_PARAMETER

Base subroutine to readout a parameter value, needed by sSDCONFIG_RD_LB.

D.26 sSDPROC_WR_LB

Called by sSDPROC_WR (see section 8).

This procedure will include the S9053 hot to cold transition. Not implemented yet.

References

1: A. Kounine, Initialization of JINF-E and JINF-R nodes, 30.6.2009,
http://ams.cern.ch/AMS/DAQsoft/JINFER_note.pdf

2: A. Kounine and V. Koutsenko, Flight software for xDR and JINx nodes in AMS-02, 30.7.2009,
http://ams.cern.ch/AMS/DAQsoft/daqsoft_note.pdf

3: P. Azzarello, 3.3 V management of the tracker crates, 18.10.2009,
https://twiki.cern.ch/twiki/pub/Main/AmsTrackerJinf/TPDS9053.pdf

-- PhilippAzzarello - 24-Aug-2010

This topic: Main > AMSTrackerJinfCode20100803
Topic revision: r2 - 2012-05-14 - MatteoDuranti