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The Buffer Control Chip (BCC)

The BCC chip receives as input the main BCO clock @40 MHz and it can deliver a 80 MHz DCLK. It then multiplexes the data coming from the two columns of one hybrid onto a 80/160 MHz data line (depending on the DCLK frequency selected, 40/80 MHz). The BCC has a 5-bit hardware address and one can perform read/write operations on its 16-bit configuration register. The BCC also receives a L1R signal which is de-multiplexed into the reset (RESETB) and trigger (L1) signals to be delivered to the ABCN chips. After a power-reset, the chip is disabled for 512 cycles of the BCO clock.

Some documentation and related links:

- BufferControlChip
- BCC-Thesis.pdf

BCC configuration

bit	Meaning
15	unused
14	80MHz BCO
13	Constant Data Mode
12	-
11	-
10	DCLK enable
9	BCO enable
8	ACLK enable
7	DCLK invert
6	BCO invert
5	ACLK invert
4	SCLK invert
3	80 MHz readout select
2	Quad mode select
[0,1]	Data MUX select source

BCC boards

-- SergioGonzalez - 28-Jun-2011

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