FPGA

Questions

- LVDS ... don't we need to consider the common voltage so seriously?
    - Si5341 ... 1.8V
        - Common mode (CM) voltage (VDDO=1.8V) : 0.9V
            - Register of CM is 0x3E (0x0114 etc) but it could be 0x3D ? (see Table 11).
        - Swing : 430mV, it means the width of diff V is 860mV.
    - SY89833ALMG ... 1.2V
        - Common mode voltage : 1.2V
        - Swing : 325mV, it means the width of diff V is 650mV.
    - FPGA
        - GXB bank ... 1.03V for both SY89833ALMG and Si5341
        - GIO bank ... 1.5V for REFCLK_125M (SY89833ALMG), 1.8V for REFCLK_VAL_P0 (Si5341)

Tips

- In the DDR3 memory simulation, it is better to use ModelSim instead of Questa.
- Nios II Command Shell
    - We can find it in the Windows's menu (Go to the left-buttom of your Windows PC).
    - https://service.macnica.co.jp/support/faq/127261 (instruction_master and data_master)
- SOPC Builder (System on a Programmable Chip Builder) --> Qsys --> Platform Designer
- PMA = Physical Media Attachment, PCS = Physical Coding Sublayer
    - PMD - PMA - PCS : Physical layer of OSI model
    - Our Gigabit Ethernet Transceiver (KSZ9031MNX) includes PMA and PCS, so that we need only MAC in FPGA.
        - MAC is in the Data Link layer of OSI model.
- FMax
    - http://www.altima.jp/column/fpga_edison/13i-Timing1.html
    - My image : Arria10 -> the max of FMax is around 1.5GHz.
- ADME = Altera Debug Master Endpoint
    - The ADME is a JTAG-based Avalon Memory-Mapped (Avalon-MM) master that provides access to the transceiver and PLL registers through the system console.
        - https://www.intel.co.jp/content/www/jp/ja/programmable/documentation/joc1445446725697/c

Iroha

- 10AX115R3F40E2SG

Arria 10 GX FPGA Development Kit

- 6XX-44366R-0G
- 10APCIe0001623
- 10AX115S2F45I1SG
- 100-0321301-E3 REV E3.1
- Si5338 U26: I2C 7A, U14: I2C 7C, Si570 X3: I2C 00

MicroPOD

- Probably 14.0625 Gbps is supported.
- RX module ... base's color is black.
- TX module ... base's color is white.

SMA cable

- Huber+Suhner GX 03272
    - ♦ 50 Ohms, 3GHz
- Amphenol 135101-R1-M0.50
    - ♦ 50 Ohms, 12.4GHz

Tools

- FLUKE 66 IR Thermometer:
  https://www.fluke.com/en-us/product/temperature-measurement/ir-thermometers/fluke-66
- FLUKE Ti95 IR Camera:
  https://www.fluke.com/ja-jp/product/thermal-imaging/thermography/fluke-ti95

Iroha Pin

- Pull up pins at FPAG (Weak Pull-Up Resistor)
    - ♦ ADD_CH[0-3]
    - ♦ USER_DIP[0-3]
        - ◊ The side of the printed ON in the physical dip-switch of the IROHA is LOW.
    - ♦ nUSER_SW
        - ◊ Push ... LOW(=GND)
- Pin info
    - ♦ nP_RESET
        - ◊ Push ... LOW

DDR3 spec

- MICRON
- MT41J128M16HA-187E:D
- VDD=VDDQ=1.5V
- 128Megx16 = 2048Meg (128M16)
    - ♦ 128M address x 16 bits = 2048M bits = 256MByte, that is, MT41J128M16HA-187E:D is 256MByte DDR3 memory (I thought that it was 2GB but this is wrong).
- 96-ball
- Timining: 1.87ns@CL7 (DDR3-1066)
- Data Rate: 1066 MT/s
- Target tRCD-tRP-CL = 7-7-7
    - ♦ tRCD = 13.1ns
    - ♦ tRP = 13.1ns
    - ♦ CL(ns) 13.1ns
- DDR3-1066 = 1066MHz = 533MHz x 2(double), up to 8.533GB/s data transfer speed
- Configuration 16 Meg x 16 x 8 banks
    - ♦ Refresh count 8K
    - ♦ Row addressing 16K (A[13:0])
    - ♦ Bank addressing 8 (BA[2:0])

        - Column addressing 1K (A[9:0])
        - DQ pins (DQ[15:0])
        - 2^14 x 2^10 x 8 x 16 = 16 x 1024 x 1024 x 8 x 16
- Mode : x8 mode
    - see https://service.macnica.co.jp/support/faq/94701, this is the case for Arria 10, I think.
        - I'm using two of x8 mode in the bank: DQ36 and DQ38.
- Pin location
    - We should run DDR3 example design to see if the pin assignment works well.
        - Read page 38 of "External Memory Interface Handbook Volume 2: Design Guidelines" (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/external-mem)
            - Search for "*_altera_emif_arch_*_readme.txt", and then read Section 6 etc (Pin locations).

PHY (network)

- KSZ9031MNX
    - PHYAD[2:0] is set to be 000 in my design but it was 011. I don't understand this reason.
        - MDIO access can be done by 0x3 instead of 0x0.
    - MODE[3:0] is 0001.
    - LED MODE = 0
    - CLK125_EN = 0

Clock spec

- KC5032A100.000C1GE00
    - Jitter (peak-to-peak) = 40 ps

Comments for a next version of IROHA

- parts with a symbol of (and a symbol of) means they are not implemented.
- Polarity of micropod
- LED index should be the same order of dip switches etc on the board.
- More LED is better for debug, for example, 8 LEDs or more.
- Swap NIMOUT connections (in the 1st page) : this is my mistake.
- U40 (Current monitor) and U41 were removed (by Ikeno-san) due to a wrong design. We need to fix the design.
    - Wrong pins in U41
- U7 (Ethernet) : R33 and R34 was re-connected to 1.8V (by Ikeno-san).
    - According to Ikeno-san, this tip has a bug, where there is no plan to fix it by its provider.
- Reset switch is not stable.
    - We might use 1.8V instead of 3.3V for VDD and SENSE.

Test04 (under IrohaArria10/@HP Note PC)

- LED, Dip switch check
- Clocks
    - 100M clock (originally for DDR3) with DSP (IO PLL Intel FPGA IP) ... done
    - 125M diff-clock cannot be used yet.

Test06-DDR3 (under IrohaArria10/@HP Note PC)

- try to use DDR3 memory but I cannot get it...
- qsf (20180817v2) was made from 20180817 by replacing emif with DDR3 and also add 1.5V info to all the DDR3 pins. However this new file cannot be read properly. I did not understand its reason. * "Clean project" can help us! This can be found in "Project".

Test01 (under IrohaArria10/@Desktop PC)

- LED, Dip switch check
- It works well.

Test02 (under IrohaArria10/@Desktop PC)

- Nios II but it does not work.

Test03-DDR3 (under IrohaArria10/@Desktop PC)

- DDR3 memory but it does not work. -> It worked well (it means that the Fitter worked well. It does not mean that we can read/write data to/from DDR3 memory).
    - ♦ emif_0_example_design_v3/qii/ed_synth/
- Jan 2019: emif_0_example_design_v3/sim/ed_sim/mentor/
    - ♦ Simulation with ModelSim DE 10.6e worked well.
        - ◊ Producedure
            - · Run ModelSim, Change directory (from "File" menu) to emif_0_example_design_v3/sim/ed_sim/mentor, do "source msim_setup.tcl" and "ld" (or "ld_debug"), then "run -all" in the Transcirpt window.
            - · Some waves will be changed and we can see some messages in the Transcript window from around 95us. About 280us was simulated in case of "Skip calibration".

```
#           --- SIMULATION PASSED ---
# ** Note: $finish    : ./../altera_emif_sim_checker_180/sim/altera_emif_sim_checker.sv(230)
#    Time: 279455890 ps  Iteration: 4  Instance: /ed_sim/sim_checker
```

- Jan 2019: emif_0_example_design_v3/qii/ed_synth
    - ♦ EMIF parameters
        - ◊ Used values from a DDR3 ref note (Micron) as much as possible.
        - ◊ 400MHz is used. PLL becomes 100MHz.
            - · If I set it to 533MHz, PLL becomes 133.25MHz (=533/4).
                - Even if I used 533 and 133.25 in the setting but 100MHz as a real clock, I got 1010 (LEDs).
    - ♦ Compiled with ed_synth.qsf (see name and location of pins of DDR3 etc).
        - ◊ nUSER_SW (PIN_AU20) as global_reset_reset_n.
        - ◊ oct_oct_rzqin is connected to PIN_G16 (100 Ohm) but I don't if this is correct.
    - ♦ I saw the next result in IROHA's LED (1010):
        - ◊ emif_0_status_local_cal_success ... LED on
        - ◊ emif_0_status_local_cal_fail ... LED off
        - ◊ emif_0_tg_0_traffic_gen_pass ... LED on
        - ◊ emif_0_tg_0_traffic_gen_timeout ... LED off
- https://www.intel.com/content/www/us/en/programmable/support/support-resources/knowledge-base/solutions
    - ♦ Termination logic option is set to Differential for input \, but setting is not supported by I/O standard <single-ended I/O standard>

        - Change PHYS Clock in IP
- ~~I used ARRIA_10_RF40_4_20180825DDR3try1-removeunused-forAlteraExample-renamedToDDR3 but it did not worked well.~~
- ~~I tried to fit DDR3 several times by changing pin assignment. However this was not an failure reason. By removing one of "always", the fitter did work well. I don't know its reason.~~
- EMIF example
    - I made an example by using qsys.
    - I followed the next video:
        - https://www.youtube.com/watch?v=QV77CrTBAaI
    - https://www.youtube.com/watch?v=chmiGrXUxVs

Test04-DDR3 (under IrohaArria10/@Desktop PC)

- The purpose of this dir is the same as Test03-DDR3 but this has an example dir.
- DDR3 memory but it does not work.
- emif_0_example_design_qii/ed_synth
    - Can do "Fitter" etc w/o any error (using the default example code) ... setting A
    - Then, constraint pins with ARRIA_10_RF40_4_20180825DDR3try1-reassign-removeunused-forAlteraExample but pins assignment is the same as the "setting A". -> worked well.
    - Then, constraint pins as IROHA with ARRIA_10_RF40_4_20180825DDR3try1-removeunused-forAlteraExample. -> worked well.
        - In both, I removed "set_instance_assignment -name IO_STANDARD "1.5 V" -to emif_0_pll_ref_clk_clk".
            - For ARRIA_10_RF40_4_20180825DDR3try1-reassign-removeunused-forAlteraExample I also removed the pin setting of emif_0_pll_ref_clk_clk.
            - For ARRIA_10_RF40_4_20180825DDR3try1-removeunused-forAlteraExample, I tried both (the pin setting of emif_0_pll_ref_clk_clk is set or not) and both of them worked well.

Test05-GXB (under IrohaArria10/@Desktop PC)

- References
    - https://service.macnica.co.jp/support/faq/121865
    - https://service.macnica.co.jp/support/faq/121665
- "Basic (Enhanced PCS)" might be needed for high speed link like 10Gbps but I cannot use it because P/N pins are inversed in some GXB pins.
    - When I designed PCB, I thought that we can swap polarity by using IP core etc but this is the case for "Basic (Standard PCS)", which is 4Gbps or slower. Anyway I use this mode at the moment.
    - I swaped P/N polarity by using tx_polinv and rx_polinv (12'b100110011001).
    - https://www.intel.com/content/www/us/en/programmable/support/support-resources/knowledge-base/s

Test06-CLK (under IrohaArria10/@Desktop PC)

- converted LVDS clocks to the single-end signal clock (helps from Nicolas).
    - Use the next 2 lines
        - set_instance_assignment -name IO_STANDARD LVDS -to REFCLK_125M_P
        - set_instance_assignment -name INPUT_TERMINATION DIFFERENTIAL -to REFCLK_125M_P
- qsf file

- DON'T constraint _N pins in this file. This is very important! I need to fix my qsf.
- Also, it is better to constraint only PINs I use for each design (first).

Test07-ValCLK (under IrohaArria10/@Desktop PC)

- Si5341A-D-GM
- Reference pages
  - http://www.picfun.com/f1/f06.html
  - https://sites.google.com/site/de0defpga/verilog-hdl/i2cbasumasuta-i2c-bus-master
  - http://sudoteck.way-nifty.com/blog/2010/06/i2c-read-d57b.html
- i2c_interface_SI5341A.v and Set_SI5341A_OnePage.v
  - 2 test versions
  - This can read/write 0xFF at the register of 0xFF.
- Set_SI5341A
  - a full version
  - This can read/write 0xFF at the register of 0xEEFF, where 0xEE is the page of the register. This is controlled by 0x0001.
- I can read the register and it looked OK.
  - ex) 0x74 can be seen in the register of 0x000B.
  - I did several checks for read/write. They looked OK.
  - A WRITE-READ test using 0x0018, 2M clock (the value of this register is 0xFF)
    - write 0xF0 and then read soon. It was 0xF0.
    - after a few 10 min (w/o power off), I tired to read it again. It was 0xF0.
    - then, power off. Then I read it again. It was 0xFF.
- However, I cannot see 100MHz etc clock at the OUT6.
- Clock configuration
  - Test07-ValCLK/ClockSettingsFiles
    - CONF1 ... 100MHz (OUT6) etc
    - CONF2 ... 200MHz (OUT6) etc
- Clock for I2C
  - 2MHz clock is accepted. (I don't know if this is OK but it looked to work well.)
    - The value of the clock is for the argument of this module. This is not a real SCL clock.
    - SCL clock is around one 3rd of the given clock, for example, in case of 2M clock, SCL clock is around 700MHz.
  - I also tried to use 1.2M clock, which might be close to 400kHz I2C. But I did not test the setting with this clock so much. After that, I have used 1.2MHz as default and several checks were did but I cannot see 100MHz clock like 2MHz.
  - I also tried to add many mode_i2c to decrease clock less than 100kHz (this is a standard I2C) but I cannot see 100MHz clock.
- Checks with oscilloscope
  - Pins looked OK.
  - FINC was set to 0 in Quartus but the situation did not change (100MHz cannot be made...)
    - I don't need to use this pin (probably I can also do 0x0339 to 0x00.).
  - A pulse of the 48MHz oscillator is not so good. It could be one of reasons why we cannot make clocks... (this is my guess.)

Test08-Nios (under IrohaArria10/@Desktop PC)

- Section 5 of FPGA Altera Book
  - https://service.macnica.co.jp/library/113961
  - https://service.macnica.co.jp/library/114097
  - https://qiita.com/daxanya1/items/917c92ec6c642bd8e9b5

- ♦ https://service.macnica.co.jp/support/faq/115129
- ♦ http://fpga.seanwrall.com/lessons/lesson2/
- ♦ A simple NIOS2 program worked: LED is changed according to dis-switch.
  - ◊ First step
    - · NIOS2 block was made by using "Platform Designer" (its old name is Qsys).
      - I used NIOS2, PIO for INPUT (dip-switch, 4bits) and OUTPUT (LED, 4bits), On-Chip memory, JTAG uart, Sysid.
        - ♦ Base address -> Use "System -> Assign Base address" tool.
  - ◊ Second step
    - · Made a top level program in Quartus. (Test08.v) This is very simple.
  - ◊ Third step
    - · Made a NIOS2 program by using "Nios II Software Build Tools for Eclipse". This is also simple.
      - Made a workspace.
      - I used "Hello World Small" as a template but all the initial code was deleted.
      - IORD_ALTERA_AVALON_PIO_DATA(PIO_1_BASE) etc must be used.
  - ◊ Run
    - · Load Test08.v program to FPGA by using Programmer at Quartus.
    - · "Run" or "Debug" NIOS2 at Eclipse.

- Also I tried to run QuestaSim.
  - ♦ https://service.macnica.co.jp/library/110605
  - ♦ http://www.lab3.kuis.kyoto-u.ac.jp/~ktakagi/le3a/flow/simulation.html
  - ♦ QuestaSim path
    - ◊ Tools -> Options -> EDA Tool Options -> C:\questasim64_10.7b\win64 for QuestaSim
  - ♦ To make a testbench, use "Assignments -> Settings".
    - ◊ EDA Tool Settings -> Simulation
      - · Select "Compile test bench", and select vt file, which must be made with an empty before, for example, testbench08.vt under */simulation/modelsim/
      - · Then, Processing -> Start -> Start Test Bench Template Writer
      - · Edit the testbench08.vt file.
    - ◊ Run simulation from Quartus
      - · Tools -> Run Simulation Tool -> Gate Level Simulation, then QuestaSim window is opened by Quartus.
      - · If you see Error (#Error loading design), try to "Recompile" *tst file of "work" in the "Library" window at QuestaSim. Click the right button and select "Recompile".
      - · By using QuestaSim, run simulation: Simulate -> Start Simulation. A new windows is opened by QuestaSim. Then select gate_work/*tst (or work/*tst, probably they are the same) and click OK.
        - We can open a "Wave" window from the "View" menu.
        - We can save signal lines used in the Wave window, then we can load it next time.

Test09-GXB(-tryX) (under IrohaArria10/@Desktop PC)

- Info from Nicolas: https://fpgawiki.intel.com/wiki/High_Speed_Transceiver_Demo_Designs_For_Current_and_Older_Families#A
  - ♦ I used 4-lanes Arria10 GX PCIe Development Kit from the "Transceiver Toolkit Designs"
    - ◊ Assmerbler: Can't use configuration device EPCQL256 with selected programming mode (in Quatus 18.0)

· See https://forums.intel.com/s/question/0D50P00003yyTHPSA2/assmerbler-cant-use-conf
- remove set_global_assignment -name USE_CONFIGURATION_DEVICE ON from the qsf file.

- I tried to make a similar one with 3 links (P[1], [2], [5] which have a correct polarity).
  - I used ARRIA_10_RF40_4_20180920_simple.qsf.
  - Error (14566): The Fitter cannot place 3 periphery component(s) due to conflicts with existing constraints (3 HSSI_PMA_TX_BUF(s)). * I tried to make the same but new project from scratch (-try2) to avoid this error but it was not successful.

Test09-GXB-VHDL

- I did copy and paste from 12-lane's VHDL code from the example used in Test09-GXB. It looked to work well. I need to understand what is different from Verilog.
  - ARRIA_10_RF40_4_20180920_simple12_VHDLTest.qsf
- Why cannot we see the polarity issue?
  - Not sure but probably the BER test trasmit data one-lane-by-one-lane.
- Current monitor
  - By adding one-lane test, around 0.01V increased.
  - Test1 case
    - ◊ Switch off 0.04A, Switch on 1.03A (3 pairs of microPOD are connected with TX-RX cables.), Fireware load 1.48A, Then 1.52A after doing some tests, 12-lanes BER test 1.62-1.63A, Turn off 12-lanes BER test 1.52A.
    - ◊ Before having 3-pairs, I ran the same Firmware with only 1-pair and I saw large BER in lane 9 or 10 (I don't remember it) but after having 3-pairs, I did not see such relatively large BER in any lane of 12-lanes (I did not use 36-lanes.).
      - · I don't know its reason but the physical connection was improved?
      - · 2E10^13 or more in all the lanes (12) and I saw 1 BER in the lane 6 (BER=4.7E10^-14).

Test09-GXB-VHDL-SMA

- ARRIA_10_RF40_4_20180922_SMA_VHDLTest.qsf
- REFCLK_UPOD0_P (PIN_AE7, Bank 4F) cannot be used for SMA, which are in Bank 1H (PIN_E33, PIN_A37).
- REFCLK_UPOD2_P (PIN_N33, Back 1G) can be used by using x6/xN feature (as far as I understood).
  - xN Clock Line: xN Up/xN Down can access the neighbor banks. MCGB (Master CGB) ports of ATX PLL can be used.
- SMA cable = GX 03272
  - 6Gbps : BER = 0 with 10E^12
  - 12.5Gbps: BER = 1.55E^-2
- SMA cable = 135101-R1-M0.50
  - 12.5Gbps: BER = 1.55E^-2

Test09-GXB-VHDL-MultiPODs

- Try to use 3-pairs of MicroPOD simultanously.
- First I tried 3-pairs but it did not work: Firmware was complied and fitted well but the ecorizer(?) cannot be identifiled.
  - "FOR i IN 0 to (NUMBER_OF_XCVR_LANE-1) GENERATE" was used to use 3-pairs.
  - I knew that the 3rd MicroPOD receiver (MircoPOD2) was breaken when we tried to fix other issue.

        - I think that we can use its tranceiver.
- Second I tried 2-pairs (MicroPOD0 and MicroPOD1) and it worked well.
        - "FOR i IN 0 to (NUMBER_OF_XCVR_LANE-2) GENERATE" was used to use 2-pairs.
        - Compile a firmware, and then run "Transceiver Toolkit" from Tools, System Debugging Tools menu of Quartus.
        - Current: load firmware 2.06A, run 24-lanes test 2.30A --> around 0.01A per lane
        - BER: 1E^13 or more in all the lanes (24) at once and I saw 3 non-zero BER lanes: MicroPOD0 lane 2 BER = 9.0E^-13, lane6 BER = 1.7E^-11, MicroPOD1 lane 8 BER = 1.3E^-8
- Jan 2019
        - I used Si5341 as Clock for MicroPOD.
                - 125MHz ... A test with the Transceiver Toolkit worked well. ("Locked")
                - 300MHz ... Not works (not locked)
                - 126MHz ... BER. It sometimes became non-locked. Unstable.
                - 156.25MHz ... BER. It sometimes became non-locked. Unstable.
                        - Even if I changed ATXPLL's clock to 156.25MHz (from 125MHz), it was unstable. (unlocked somtimes...)

Test10-CLK-I2C

- Used Open Core's I2C program but the situation was not improved.
        - The observed result is the same as Test07-ValCLK.
- 2019 Jan
        - I found my mistake, that is, we need preamble and post configutions to change the register's values.
                - I thought that such configurations are needed only to change the default values. (I realized that some parameter values are different to do it.)
                - I introduced a 10ms wait time after power on.
                - I added 300ms wait time as suggested by Clock Builder application.
        - I checked 9 outputs with osciloscope. They are OK in term of freq but the shape is not so good (for me) but it should be OK, they are small swing around V= ~ +0.9V. This is LVDS.
                - 300MHz (MOV_0956), 625MHz (MOV_0955), 644.53MHz (MOV_0954) outputs are not good because strange behaviors were observed in a simple LED test program.
                        - MOV_0954 and 0955... I expected that LED moves (no-blink LED moves L to R) with about 0.9 sec's step but this was not.
                        - MOV_0956 ... LED moved with an opposite direction. I don't understand it.
                        - 300MHz, 625MHz, 644.53MHz seems to be small width (?) ~0.9V (max), which is difference between P and N.
                - LOLb was H for both CONF05-2 and CONF06.
        - LOLb ... Status pin (H is "PLL is locked", that is, good status. L is out-of-lock, that is, bad status.)
        - FINC ... I don't use it. This is a pin to change feq according to register values.
        - OUT6 (REFCLK_VAL_P0) is connected to a standard FPGA bank but others (8 OUTs) are connected to GTX banks.
        - I made Si5341_I2C.vhd to use this clock in other projects.

Test11-NIM

- NIM IN
        - I connected NIM IN to LED. I inputed 1Hz NIM pulse (-0.7V or -0.8V), whiich was generated by AFG 2105 function generator.
                - Two NIM input pins worked well. I can see blinking of LED up to 20Hz by my eyes.
                        - High feq should be tested by other ways in future.

◊ -0.7V/-0.8V -> Red of LED, 0V -> null on LED

- NIM OUT
  - ♦ When I don't do anything but turn on IROHA, two NIM out pins output -0.8V.
    - ◊ When I switch off IROHA, two NIM out pins is 0V.
  - ♦ Strange

FPGA N0	0	0	1	1
FPGA P0	0	1	0	1
NIM OUT0	-0.8V	-0.8V	0V	-0.8V

FPGA N1	0	0	1	1
FPGA P1	0	1	0	1
NIM OUT1	-0.8V	0V	-0.8V	-0.8V

- ♦ I used these pins as standard pins not LVDS.
- NIM OUT
  - ♦ I specifies pins as LVDS. (LVDS and Diff) as follows:
    - ◊ set_instance_assignment -name IO_STANDARD LVDS -to NIM_DOUTP0
    - ◊ set_instance_assignment -name INPUT_TERMINATION DIFFERENTIAL -to NIM_DOUTP0
  - ♦ Still strange (but solved!)
    - ◊ When I don't do anything but turn on IROHA, two NIM out pins output -0.8V.

FPGA P0	1	0
NIM P0	1	0
NIM OUT0	-0.8V	0V

FPGA P1	1	0
NIM P1	0	1
NIM OUT1	0V	-0.8V

- ♦ I found that in the 1st page of our Kairo-zu, NIM_DOUTP1 and NIM_DOUTN1 are swapped!

Test12-NIC

- RJ45 Socket : 0826-1A1T-23-F
  - ♦ The front LED parts (this is just a kind of light guide) are connected to the backend LED parts.
- RJ45_LED1 (GREEN) and RJ45_LED2 (YELLOW)
  - ♦ 1 in the firmware ... LED = ON
  - ♦ 0 in the firmware ... LED = OFF
  - ♦ When we turn IROHA on, both LEDsare on.

Test13-NominalDDR3

- Just to make example EMIF codes for different DDR3 settings.
  - ♦ emif_0_example_design: IP name = DDR3, default parameters with 2GB (128MB x 16), CL7
    - ◊ Questa ... infinite loop (?) in step 3
  - ♦ emif_0_example_design_DDR3_Default: IP name = DDR3 default, default parameters
    - ◊ Questa ... infinite loop (?) in step 3

Test14-NominalDDR3_Ver15

- Use Quartus v15.0

Test15-NIC2

- https://qiita.com/homelith/items/a80a5e4d45ea9280145a

Test15-NIC2-ALTDDO_OUT-CycloneV

- To make ALTDDO_OUT by using GPIO for Arria10, I made ALTDDO_OUT with CycloneV and converted it (see ug_altera_gpio.pdf).

Test16-DDR3

- Try to make a firmware to use DDR3 via NIOS II.
    - ♦ Used Verilog. Pin assignment (fitter) was failed.

Test17-DDR3

- Try to make a firmware to use DDR3 via NIOS II.
    - ♦ Used VHDL. Pin assignment was failed.
- We may need to consider how to contraint circuits? Indeed if I removed PLL, I was able to do the fit by Fitter.
- I used 125MHz as a clock for Clock Source.
    - ♦ I used a timining analzier to constraint input clocks : 125MHz and 100MHz.
        - ◊ https://service.macnica.co.jp/library/111585
- On-chip memory might work in case of a small memory range but when I used a larger range, NIOS II looked to be crashed (no responce).
    - ♦ This is because I overwrite NIOS II code, which was loaded to a part of On-chip memory, for example, 0x1000_8000 - 0x1000_9xxxx.
    - ♦ So, when I used memory of 0x1000_a0000 or later, NIOS II did not crashed.
- NIOS II
    - ♦ See the above Test08-Nios. We can find web sites, which explain how to use NIOS II.
        - ◊ Update BSP (after its configuration or Quartus code) : select "BSP Editor..." from "NIOS II" in the menu, which is shown when I click the right bottom of mouse on the name (shown in the Poject Explorer) (with _bsp).
        - ◊ Compile my codes : select "Build Project" in the menu, which is shown when I click the right bottom of mouse on the name (shown in the Poject Explorer) (without _bsp).
        - ◊ Run NIOS II : select "3 NIOS Hardware" from "Run As" in the menu, which is shown when I click the right bottom of mouse on the name (shown in the Poject Explorer) (without _bsp).
    - ♦ We can use memtest_small.c, which can be found in "Test17-DDR3/software/nios_test1/". This might be opened if we open "Test17-DDR3/Nios2-workspace" as workspace, which might be asked when we run Eclipse.
- LATOME's pin of DQ and DM is OK (fitted).
- IROHA's pin of DQ and DM is OK (fitted). [@CERN, March 2019]
    - ♦ 400MHz not 533MHz was used.
    - ♦ Scatter-Gather DMA: mem-to-mem
        - ◊ Nios II workspace: Test17-DDR3/Nios2-workspace3
        - ◊ Nios II code: Test16-DDR3/sotware/ddr3_test6, try to use sidma3() ... it looked to work well.

        - Nios II's memtest_small.c
            - Nios II workspace: Test17-DDR3/Nios2-workspace4
            - Nios II code: Test16-DDR3/software/ddr3_mem-test-small1
                - 256M bytes: 0x1000_0000 - 0x1fff_ffff is OK.
- Nios II
    - Once I'll make a new application (from normally a template),
        - run "Nios II -> Generate BSP" from X_bsp.
        - run "Build Project" from X.
        - run "Run Configurations...", then make New_configuration by double-clicking "Nios II Hardware".
            - At the "Target COnnection" tab, I selected 5 checks: Ignore mismatched system ID, timestamp, Download ELF, Start processor, Rest the selected target system".
    - If I want to change memory where I put my firmware, edit "Linker Script" tab by using "BSP Editor..." from X_bsp.

Test18-NIC (CERN)

- NIOS II
    - Error of "Verify failed between address 0x2000000 and 0x200FFFF"
        - 1) At Platform Designer (Qsys), change "sysid_0" to "sysid"
        - 2) At Platform Designer, Nios II's debug_reset_request output should be connected to reset of other components except PLL and "Clock source".
        - 3) At Eclipse, at Run Configuration, check on on "Reset the selected target system" of Target Connection.
        - 4) Re-connect UBS cable.
        - 5) Reduce the size of onchip memory.
- https://forums.intel.com/s/question/0D50P00003yyQTESA2/cyclone-iv-gx-dev-kit-getting-ethernet-to-work?la
- Clocks
    - clk (clk_clk) ... 50MHz, tx_clk ... a clock for MAC registers
    - rx_clk (eth_tse_0_pcs_mac_...) ... 125MHz ... a clock for GMII
    - ff_tx_clk and ff_rx_clk (eth_tse_0_transmit/receive_...) ... 100MHz ... a clock for Avalon-ST
        - I used 3 clocks generated from a single PLL. Also I used the same clock for ETH_GTX_CLK (125MHz).
        - When I used ETH_RX_CLK (it might be 125MHz), my IP cannot be SW_RESET.
- Loopback
    - Local loopback
        - https://forums.intel.com/s/question/0D50P00003yyMbkSAE/tse-with-sgdma-in-loopback
        - PROMIS_EN should be 1 to recieve data from transmit in the loopback mode.
- SGDMA (Scatter-Gather DMA)
    - https://forums.intel.com/s/question/0D50P00003yyKQCSA2/memorytomemory-sgdma-problem
    - https://forums.intel.com/s/question/0D50P00003yyNKESA2/nios-ii-data-cache-problem
    - Use uncached memory. Perform "alt_dcache_flush_all()" in the present NIOS II version.
        - find and see HAL API Reference in the internet.

GMII

- Gigabit Media Independent Interface for 1000Base-T
    - MII ... Media Independent Interface, this is for 100Base-TX and 10Base-T
- Image
    - Network - RJ45 connector - PHY chip - FPGA (MAC) -
        - "RJ45 connecor - PHY chip" = Layer 1
        - "FAPG (MAC) -" = Layer 2

I2C - USB board

- HidSmbus Example (Windows application name)
    - https://jp.silabs.com/products/development-tools/interface/cp2112ek-evaluation-kit
    - Since I use 0x74 as Si5341 Clock I2C slave address, 0xE8 must be used in this software to access I2C line.
        - 0x74 is a 7 bit code, then we need to add 0 in the lowest bit to make a 8bit code.
    - J7 ... I connected 1.8V (external 1.8V applied at H1/TB1) to the middle pin of J7.
    - J8 ... any configuration seems to be OK.
    - I can read the memory by using I2C when I don't write a firmware to the Si5341.
        - 0x02 ... 41, 0x03 ... 53, 0x04 ... 00, 0x05 ... 03 etc
        - 0x0B ... 74 (Slave address with 7 bits)
        - 0xE2 ... 03 (it means that we still have 2 regions to write registers's values permanently. See section 8 of Si5341-40-RM.pdf.)
            - So far we don't need to change the default register's values.
    - After I wrote a firmware to the Si5341, 0x00 is returned. It means that we cannot access register by this board once we write a firmware.
        - Z (Hi impedance) is set for I2C Clock and Data by firmware but we cannot access.
    - I tried to write register values by using HidSmbus application but I cannot do it. I think that this is a feature of this application.

Configuration (Flash memory)

- AS configuration
    - AS = Active Serial
    - Iroha uses AS x 4 mode.
    - MSEL[2..0]
        - AS x1 and x4 : Power on reset (POR) delay with Fast ... 010, Standard ... 011 (1.8V), Note LATOME uses 011.
    - CLKUSR (AM24 pin) = 100MHz (already set)
- Serial Flash Loader Intel FPGA IP core
    - AN370 2017.12.18 version
- https://forums.intel.com/s/question/0D50P00003yyRG2SAM/how-to-use-serial-flash-loader-in-quartus-ii-if-al
    - Concerning item 7, I used 10AX115R3.
    - Concerning item 12 and 13 in this page (intel page), I found two FPGA (one is 10AX115R3F40 and the other is 10AX115R3). I deleted the former one, and then I checked v in the Program/Configure for both FPGA and EPCQL1024.
- Iroha has MT25QU01GBBB8E12-0SIT, which is MT25Q is a high-performance multiple input/output, 1Gb, 1.8V, SPI Flash memory device: EPCQL1024.
- How to erase an image from the flash memory
    - https://service.macnica.co.jp/support/faq/91937
    - I deleted FPGA which is shown first when I ran the programmer. Then, I added FPGA (10AX115R3) and added Flash (EPCQL1024). Then select "Erase" and click "Start".

Signal tap II

- How to keep or preserve registers to monitor by the Signal tap II.
    - http://forum.macnica.co.jp/t/topic/1144
        - VHDL ... use attribute dont_merge or preserve
        - Verilog ... synthesis dont_merge etc.
        - BUT it did not work well...

This topic: Main > FPGAMemo
Topic revision: r78 - 2019-03-12 - JunichiTanaka