2012-10-15, hazen

New firmware from Drew with 16-bit counter substituted for payload here: MCS file. Try it in top/bottom of one HTR in slot 12. Bottom (spigot 1) looks pretty good but Top (spigot 0) has problems (EvN corruption, UERR and CERR seen).

So far all but spigot 0 look OK with histogramming firmware. Try normal firmware in slot 12 for run 6. Problem remains with spigot 0, so tentatively conclude there is a hardware problem.

Now try 14500 (real histogramming FW) in slot 14. Disable spigot 0. So, we have:

- Spigot 1 - normal FW
- Spigots 2, 3 - couter test FW
- Spigots 4, 5 - 14500 FW
- Spigots 6, 7 - normal FW

Notes	DCC Status	Binary file	Hex dump
Run 4 - histo firmware in spigots 0, 1	DCC status	test4.dat	test4.txt
Run 5 - histo firmware 0-3, normal 4-5	DCC status	test5.dat	test5.txt
Run 6 - histo firmware 2-3, normal 0, 1, 4, 5	DCC status	test6.dat	test6.txt
Run 7 - see above	DCC status	test7.dat	test7.txt

2012-10-12, hazen

HTR firmware:

```
Map for bus  caen:0 (0): 7 HTRs, 1 Fanouts, 0 LTBs, and 1 DCCs
Slots:          9      11      12      13      14      15      16      17      18
Cards:       TTCf     DCC     HTR     HTR     HTR     HTR     HTR     HTR     HTR
S/N  :         31       0     238      18      59     261      66      16     250
fw   :          2      41      47      47      47      47      47      47      47
SWAP :       true    true    true    true    true    true    true    true    true
HTR Slot:      12      13      14      15      16      17      18
S/N(dec)      238      18      59     261      66      16     250
fwVME          47      47      47      47      47      47      47
fwTOP       14500     b90     b90     b90     b90     b90     b90
fwBOT       14500     b90     b90     b90     b90     b90     b90
```

DCC firmware:

```
>ver
DCC2 Serial# 2188
Firmware versions:
 xilinx:  0x3026  CRC: 0x0044d878
    lrb:  0x010e  CRC: 0x006bfb4b
    vme:  0x0104  CRC: 0x00410ee6
   cpld:  0x0002
FPGAs loaded: DSP(std) LRB5 LRB4 LRB3 LRB2 LRB1
LRB0 ver: 0x010e
LRB1 ver: 0x010e
LRB2 ver: 0x010e
LRB3 ver: 0x010e
LRB4 ver: 0x010e
```

Initialize HTR in slot 12 using Drew's script htr_histogram_run_TOP.htr. Issue ECR, then 10 L1A. DCC2 status:

```
>dcc/stat
0000 [00000000]:
TTS: 1000 RDY
0004 [30260001]:  run mode
0008 [00000000] (spy prescale)  0018 [00000000] (sych ctrl)  0080 [00000000] (page) [000003c6] (m
0088 [3f603f70] (ttc)   [0001000f] (slink)
        HTR mis:  009 009 009 009
        HTR blk:  009 009 009 009
       HTR word:  dda dda 2ac 2ac
       HTR Cerr:  007
       HTR Uerr:  005
    L1A EvN mis:  009 007
    L1A BcN mis:  009 009 009 009
    L1A OrN mis:  009 009 009 009
    L1A Skipped:
     L1A Padded:
    HTR CRC Err:  005
              RDY on: 00000000 1b385d45                BSY on: 00000000 00000000
              OFW on: 00000000 00000000                SYN on: 00000000 00000000
              RUN on: 00000000 1b3880fd
           L1A Trig: 0000000a          Events Built: 00000009
        SLink Events: 00000000            VME Events: 00000009
            Cal Trig: 00000000
     L1 EvN Mismatch: 00000009       L1 BcN Mismatch: 00000009       Bunch count err: 00000000
     Rule 5 violated: 00000000
HTR   :  OW BZ EE RL LE LW OD CK BE
HTR  0:  -- -- -- -- -- -- 09 -- -- -- -- -- -- -- --
HTR  1:  -- -- -- -- -- -- 09 -- -- -- -- -- -- -- --
HTR  2:  -- -- -- -- -- -- 09 -- -- -- -- -- -- -- --
HTR  3:  -- -- -- -- -- -- 09 -- -- -- -- -- -- -- --
```

-- EricHazen - 12-Oct-2012

This topic: Main > HTRHistogramTesting2012
Topic revision: r2 - 2012-10-15 - EricHazen