

AMS02 DAQ Framework

Analog signals from the Tracker are digitized and compressed in the Tracker Data Reduction boards (TDR). The next node in the data acquisition (DAQ) tree system, the JINF, receives data from up to 24 TDRs. In the JINF, the data from the TDRs are collated, buffered and sent to the top level JINJ boards. Then JINJ collates, buffers and passes data to the JMDC, the Main DAQ Computer. The JMDC receives the complete event and monitors the detector performance. The events are then buffered and sent out the HRDL (High Rate Dynamic Link) when they become available.

Tracker electronics is constituted by 8 crates called T0, T1, T2, T3, T4, T5, T6 and T7. Each crate contains 24 TDRs managed by 2 JINF (A and B). JINFs are doubled for redundancy (they are usually called *brothers*). All the 8 operating JINFs are read out by the JINJ. There are 4 JINJs, but only one is strictly needed for the whole DAQ system. In the Tracker, however, the redundancy is not complete:

- JINJ-1 and 2 are connected with JINF-T-A
- JINJ-0 and 3 are connected with JINF-T-B

The data are then collected by JMDC and sent to the HRDL. The actual implementation of the two HRDL lines is given by two computers. Here the actual configuration (which may change) is:

- HRDL-A --> means pcgsc00 used --> eas:hrdl pcgsc00 in the Lebedev style programs and in the slowconf.conf (SLOWGUI & AMSWire)
- HRDL-B --> means pcgsc02 used --> eas:hrdl pcgsc02 in the Lebedev style programs and in the slowconf.conf (SLOWGUI & AMSWire)

The JINJ Slaves

Dec address	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Hex address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
Crate	T2	T3	U1	T0	S1A	S1B	S0A	S0B	U0	T1	R0	R1	E0	E1	JLA	JLB	T4	T5	S2A	S2B	S3A	S3B	T6	T7

The AMS Tracker Rosetta's Stele

Crate	X	Y	Z	OCT	JINJ		JMDC				
					ADDR	NUM	A	B	P	S	
T0	+	WAKE	+	1	0x033f	03	0xA6	0xA7	0xA8	0xA9	
T1	-	WAKE	+	2	0x093f	09	0xAA	0xAB	0xAC	0xAD	
T2	-	RAM	+	4	0x003f	00	0xAE	0xAF	0xB0	0xB1	
T3	+	RAM	+	3	0x013f	01	0xB2	0xB3	0xB4	0xB5	
T4	+	WAKE	-	5	0x103f	16	0xB6	0xB7	0xB8	0xB9	
T5	-	WAKE	-	6	0x113f	17	0xBA	0xBB	0xBC	0xBD	
T6	-	RAM	-	8	0x163f	22	0xBE	0xBF	0xC0	0xC1	
T7	+	RAM	-	7	0x173f	23	0xC2	0xC3	0xC4	0xC5	

Tables with HwId, TkId, Ladder Name, etc...

The TDR numeration conventions

Our	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
Hex	00	01	02	03	04	05	06	07	08	09	0a	0b	0c	0d	0e	0f	10	11	12	13	14	15	16	17	

| Lebedev | 00-A | 00-B | 01-A | 01-B | 02-A | 02-B | 03-A | 03-B | 04-A | 04-B | 05-A | 05-B | 06-A | 06-B | 07-A | 07-B | 08-A | 08-B | 09-A | 09-B | 10-A | 10-B | 11-A | 11-B ||

This topic: Main > Infos

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