Interlock minutes held on 30th of September 2009

Present: B. Puccio, B. Todd, J. Wenninger, K. Hanke, J-L. Sanchez, J-C. Bau, E. Piselli, I. Kozsar, D. Nisbet, G. Metral, B. Mikulec.

Agenda:

1. Overview of the Beam Interlock System (BIS) (B. Puccio)
2. Software Interlock System (SIS) at the SPS and LHC (J. Wenninger)
3. Upcoming issues to be solved (B. Mikulec)

1. Presentation of the Beam Interlock System (BIS)

B. Puccio gave an overview of the BIS (see his presentation); its principle, the hardware and connectivity, the user interface, reaction time, timing in general and the BIS application. He finished with the example of the BIS for the SPS/LHC transfer lines.

The BIS consists basically of an 'AND' of all relevant system conditions leading to a beam permit only in case all conditions are TRUE. There exist different possible architectures (single controller, ring or tree architecture) and their combinations. The BIC comprises beam interlock controller boards with 14 inputs; up to 2 BICs can be installed in one VME chassis. A FESA class has been developed for monitoring and remote testing. Dedicated User Interfaces installed in the user system's rack connect the user system through a copper cable. The inputs are current loops. Always 2 independent inputs are required for redundancy; there are as well redundant power supplies provided per user interface. One more requirement for the user system is to be able to change the user permit to test the interlock chain.
Opto-couplers check if current is present at the input; if the current exceeds at least 10 mA, the user permit state is transmitted in RS485 format.

Of the 14 BIC inputs 7 can be masked by the operators (e.g. in case of error debugging), but the masking is automatically removed when the 'Safe Beam' flag becomes FALSE (condition of a 'safe' beam has obviously to be defined before, but could be for example when the beam current exceeds a certain threshold). A history buffer is available with ms accuracy.

As transmission time both for the copper cable and the optical fibres, an estimated value of roughly 5 ns/m has been mentioned.
One question to be answered is the concept of the 'Safe Beam' flag acting on the maskable interlock conditions. Is it really needed? How could it be implemented for Linac4? Would the information from the transformers be available in time to produce and transmit a 'Safe Beam' flag signal?

Assigned to	Start date	Description	State	Result	
F.Lenardon, L.Soby	2009-10-05	Estimate the time required to send the information on the Linac4 beam current to the interlock system.		The beam pulse will be sampled at 10 MHz. With the current system it would be possible to interlock the source for the following beam pulse. However this interlock would be done purely by software and is therefore not safe (this is similar to the Linac-2 watchdog). Should a hardware interlock be needed then this must be specified and discussed. As a different solution one could install TRIC cards with digital watch dogs and transform the signal to optical. To be seen.	edit

Concerning the BIS architecture, it has to be clarified if 1 BIC per operational mode will be used or a master BIC with connected slave BICs.

2. Software Interlock System (SIS) at the SPS and LHC

J. Wenninger explained the use of the SIS in the SPS and LHC (see his presentation). Ideally, a software interlock should only be used when there is no potential damage to equipment. The SIS is a generic software interlock system based on FESA and LSA. The basic structure of the SIS is a tree structure. At the bottom of the tree, simple logical parameter tests as well as more complex tests based on java classes can be made; processing of the results of these operations can continue. The output at the top of the tree is the PERMIT that can be exported to the BIS as well as to other systems (timing, alarms etc.). There is one Permit for the SPS ring and a Permit per transfer line. The SIS inhibits are also visible in the Sequence Manager (external conditions).
Acquisition of the input parameters is done via FESA (access a single FESA property field from a single FESA device; no correlation!), and the Controls middleware and can be monitored via japc. The SIS core receives timing trigger events, processes the input data and exports the Permit. The latching of the SPS interlock system is automatically reset by the SIS.

The typical reaction time of the SIS is <0.5 s (mainly dominated by cmw). In the SPS the SIS handles currently ~900 device subscriptions, ~1800 in the LHC. J. Wenninger stated that the experience of the SPS with the SIS was excellent.

3. Upcoming issues to be solved

B. Mikulec summarised a few starting points and open questions to be solved before going into greater detail.

- Evaluate which equipment can be damaged by the Linac4 beam: H0/H- dump in case of combined distributor and foil failure, septum and other magnet coils,...?
- Continue working on a timing diagram showing all important systems (see first point) with their time limitations (reaction time to identify H0/H- dump problem, source reaction time to interlock signal,...)
- Define all operational modes and the related equipment to be interlocked and make the distinction between hardware and software interlocks: this will allow taking a decision on the BIS structure and the number of BICs
- Clarify if the current interlock system for PSB/ISOLDE/beams to the PS can be maintained or if we need to adopt the BIS also there

B. Mikulec will organise a follow-up meeting in approximately 4 weeks time.

-- BettinaMikulec - 2009-10-01

- BIC-Overview_30Sept09.pdf: BIC overview
- SIS.Sept09.pdf: SIS at the SPS and the LHC
- Interlock_basics.pdf: Upcoming issues concerning the Linac4/PSB interlock system.

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