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Welcome to the XTCA web
This is the TWiki home page of the xTCA Interest Group

**Introduction**

The xTCA Interest Group has been established during the TWEPP2010 workshop in Aachen. Its mission is to further the exchange of information between developers of xTCA components (both H/W and S/W) for application in HEP experiments or accelerators. The membership is open to all representatives of non-profit organisations. Anyone who would like to join is requested to contact the convener: Markus Joos

**Meetings**

It is planned to meet twice per year; either within the framework of a suitable HEP conference or virtually via EVO.

**Past meetings**

1st meeting

September 2010 @ TWEPP2010 in Aachen. Link to contributions

2nd meeting

March 2011 @ CERN: Link to contributions

3rd meeting

September 2011 @ TWEPP2011 in Vienna. Link to contributions

4th meeting

The 4th meeting took place at CERN on Tuesday, 17 April 2012. The agenda is available here.

5th meeting

The 5th meeting took place at on Wednesday, 19 September 2012 in Oxford as part of the TWEPP conference. The agenda with presentations is available here.

6th meeting

The 6th meeting took place at CERN on 9 April 2013. The presentations are available here.

7th meeting

The 7th meeting took place during the TWEPP 2013 conference on Thursday, 26 September at 17:00. The agenda with presentations is available here.

8th meeting

The 8th meeting took place at CERN on 17 March 2014 at 14:00. An slides of the presentation are available here.
9th meeting
The 9th meeting took place on Wednesday, 25 February 2015 at 14:00 in room 4-S-30. The agenda is here.

10th meeting
The 10th meeting took place on Thursday, 10 March 2016 at 15:00 in room 13-2-5. The agenda is here.

11th meeting
The 11th meeting took place on Thursday, 29 September 2016 in the late afternoon (~16:30 – 18:30) during the TWEPP 2016 conference.

12th meeting
The 12th meeting took place at CERN on Thursday, 15 June 2017 at 15:00 in room 40-R-D10. The agenda is here.

13th meeting
The 13th meeting took place at CERN on Friday, 27 April 2018 at 10:00 in room 13-2-5. The agenda is here.

14th meeting
The 14th meeting took place at CERN on Friday, 10 May 2019 at 15:00 in room 6-2-24. The agenda is here.

15th meeting
The 15th meeting took place on Wednesday, 13 May 2020 at 15:00. The agenda is here.

16th meeting
The 16th meeting will take place on Tuesday, 11 May 2021 at 15:00. The agenda is here. Zoom: 81176881

17th meeting
The 17th meeting will take place on Tuesday, 10 May 2022 at 15:00. The agenda is here. Zoom: link.

Mailing lists
All participants will be added to the xtca-news@cernNOSPAMNOSPAMPLEASE.ch mailing list. This mailing list will be used to announce information relevant for the members of the xTCA Interest Group as well as xTCA related announcements of interest to CERN based people. In case you have problems posting mails to this list (because you don't have a CERN account) please contact one of the conveners.

Project repository
We are encouraging all participants to upload some brief information about their completed, current and future xTCA related projects to this TWiki table.

<table>
<thead>
<tr>
<th>Project name</th>
<th>Type</th>
<th>Short description</th>
<th>Status</th>
<th>Contact person</th>
<th>Institute</th>
</tr>
</thead>
<tbody>
<tr>
<td>9th meeting</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>uTCA @ DESY</strong></td>
<td>various projects</td>
<td>An overview of uTCA projects at DESY for the European XFEL</td>
<td>Under development</td>
<td>Kay Rahlich</td>
<td>DESY</td>
</tr>
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</tr>
<tr>
<td><strong>AMC13</strong></td>
<td>MicroTCA MCH</td>
<td>AMC (in MCH site) for clock/controls/DAQ functions</td>
<td>Deployed in CMS and other</td>
<td>Eric HAzen</td>
<td>Boston University</td>
</tr>
<tr>
<td><strong>APOLLO</strong></td>
<td>ATCA</td>
<td>Platform for multiple ATCA blades</td>
<td>Prototyping</td>
<td>Eric Hazen</td>
<td>Boston University</td>
</tr>
<tr>
<td><strong>GLIB</strong></td>
<td>mid size, double width AMC</td>
<td>An evaluation platform and an easy entry point for users of high speed optical links</td>
<td>Under development</td>
<td>Paschalis VICHoudIS</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>MMC_HW</strong></td>
<td>28.5 x 20.5 mm mezzanine card for AMC board</td>
<td>A mezzanine implementing the Module Management Controller functions required by the µTCA standard</td>
<td>Available (as well as a ref. design)</td>
<td>Vincent BOBILLIER</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>MMC_SW</strong></td>
<td>MMC SW for the Atmega128 the MMC mezzanine is based on</td>
<td>SW implementing the Module Management Controller functions required by the µTCA standard, including HPM.1 support</td>
<td>Available</td>
<td>Julian MENDEZ, Markus JOOS</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>GLIB_MMC_TEST</strong></td>
<td>mid size, double width AMC</td>
<td>An evaluation platform for the MMC mezzanine carried by the GLIB</td>
<td>Under development</td>
<td>Paschalis VICHoudIS</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>WR MCH</strong></td>
<td>full size, single width MCH</td>
<td>Used in the White Rabbit switch</td>
<td>Under development</td>
<td>Tomasz WLOSTOWSKI</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>MINI-T5</strong></td>
<td>full/mid size, double width AMC</td>
<td>Processing card for an upgraded Level-1 Calorimeter Trigger. Substantial connectivity: 160Gb/s optical, 64Gb/s LVDS</td>
<td>In system tests</td>
<td>Greg ILES</td>
<td>Imperial College London</td>
</tr>
<tr>
<td><strong>ALB</strong></td>
<td>mid size, double width AMC</td>
<td>An AMC load board based on the CPPM MMC that allows to control and monitor on-board dummy loads for crate power and cooling test purpose.</td>
<td>Available - In use for the evaluation tests of different uTCA crates</td>
<td>Vincent BOBILLIER</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>uTCA evaluation</strong></td>
<td>Evaluations of commercial products</td>
<td>Test various properties of commercial uTCA components</td>
<td>Under development</td>
<td>Markus Joos</td>
<td>CERN</td>
</tr>
<tr>
<td><strong>AMT</strong></td>
<td>mid size, single</td>
<td>An easy to use MMC</td>
<td>Available - In use</td>
<td>Vincent</td>
<td>CERN</td>
</tr>
<tr>
<td>Project</td>
<td>Category</td>
<td>Description</td>
<td>In system tests</td>
<td>University</td>
<td>Webpage</td>
</tr>
<tr>
<td>------------------------------------------------------------------------</td>
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<td>------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
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</tr>
<tr>
<td>width AMC</td>
<td>Test board</td>
<td>Test board for the full functionality testing of the CPPM MMC. Provides hardware access library (HAL). Modular + scalable design. Currently consists of IPBus, ControlHub and uHAL.</td>
<td>BOBILLIER</td>
<td>Webpage</td>
<td></td>
</tr>
<tr>
<td>MicroHAL</td>
<td>Firmware+Software</td>
<td>Provides Hardware Access Library (HAL). Modular + scalable design. Currently consists of IPBus, ControlHub and uHAL.</td>
<td>In system tests</td>
<td>Dave Newbold</td>
<td>University of Bristol</td>
</tr>
<tr>
<td>IPBus</td>
<td>Firmware</td>
<td>Provides firmware for R/W/RMW + Block R/W register/memory access over UDP/IP. Wishbone compatible.</td>
<td>In system tests</td>
<td>Rob Frazier</td>
<td>University of Bristol</td>
</tr>
<tr>
<td>ControlHub</td>
<td>Software</td>
<td>Provides a uniform interface between the hardware access methods (e.g. IPBus, VME, USB) and the higher-layer abstractions (e.g. MicroHAL).</td>
<td>In system tests</td>
<td>Andrew Rose</td>
<td>Imperial College London</td>
</tr>
<tr>
<td>Redwood</td>
<td>Software</td>
<td>Software layer which maps registers onto C++ objects. Can talk to the ControlHub or directly to IPBus devices.</td>
<td>In system tests</td>
<td>Bruno Soares</td>
<td>IPFN-IST</td>
</tr>
<tr>
<td>ATCA @ IPFN for Nuclear Fusion</td>
<td>Several Projects</td>
<td>Overview of several projects for nuclear fusion applications including ATCA IO boards and RTMs and a controller</td>
<td>Several completed and several ongoing developments</td>
<td>Daniel Tavares</td>
<td>CNPEM/LNLS</td>
</tr>
<tr>
<td>ABBA</td>
<td>Various projects</td>
<td>A set of boards for mastering ATCA and preparing upgrade of ATLAS LAr Back End electronics: ATCA Controller Mezzanine (hardware &amp; software) + ATCA Test Board + ATLAS LAr ROD Evaluator</td>
<td>Under development</td>
<td>Guy PERROT</td>
<td>LAPP</td>
</tr>
<tr>
<td>Sirius BPM back-end</td>
<td>double-width AMC</td>
<td>Double-width AMC with dual high-pin count FMC slots for digital signal processing, data acquisition and feedback control in ATLAS LAr ROD Evaluator.</td>
<td>Under development</td>
<td>Daniel Tavares</td>
<td>CNPEM/LNLS</td>
</tr>
<tr>
<td>MP7</td>
<td>double-width AMC</td>
<td>General purpose data processing with Xilinx Virtex-7 FPGA &amp; 740 Gbps of input &amp; output optical bandwidth</td>
<td>Available</td>
<td>Greg Iles</td>
<td>Imperial College London</td>
</tr>
<tr>
<td>JSM</td>
<td>AMC size (not AMC)</td>
<td>JTAG Switch Module for CERN Scroff / Elma crates</td>
<td>Development</td>
<td>Andrew Rose</td>
<td>Imperial College London</td>
</tr>
<tr>
<td>TwinMux</td>
<td>double-width AMC</td>
<td>Optical data concentrator with Xilinx Virtex-7 FPGA, Input: 72x1.6Gbps and 12x10Gbps, Output: 12x10Gbps</td>
<td>Prototype ready</td>
<td>Andrea Triossi</td>
<td>INFN/CERN</td>
</tr>
<tr>
<td>fwATCA</td>
<td>Slow control</td>
<td>A WinCC framework tool to automate and assist in integrating ATCA Chassis into the Detector Control Systems</td>
<td>Replaced by fwAtca for ATCA OPC UA (see below)</td>
<td>Paris Moschovakos, Robert Reed</td>
<td>CERN, University of the Witwatersrand</td>
</tr>
<tr>
<td>BCP</td>
<td>ATCA</td>
<td>Barrel Calorimeter Processor - ATCA-based front-end interface</td>
<td>Prototyping</td>
<td>Stephen Goadhouse, Nikitas Loukas</td>
<td>University of Virginia, University of Notre Dame</td>
</tr>
<tr>
<td>AtcaOpcUa</td>
<td>Slow control</td>
<td>OPC UA server for xTCA shelf managers</td>
<td>In production</td>
<td>Paris Moschovakos</td>
<td>CERN</td>
</tr>
<tr>
<td>fwAtca</td>
<td>Slow control</td>
<td>Framework component for AtcaOpcUa integration in WinCC OA</td>
<td>In production</td>
<td>Paris Moschovakos</td>
<td>CERN</td>
</tr>
<tr>
<td>fwAtcaFsm</td>
<td>Slow control</td>
<td>Framework component for AtcaOpcUa integration in ATLAS FSM</td>
<td>In production</td>
<td>Paris Moschovakos</td>
<td>CERN</td>
</tr>
</tbody>
</table>

**Other information**

- Access to PICMG standards (for people at CERN)
- MTCA.4 workshop at DESY (11 & 12 December 2012). The presentations are available here
- MTCA.4 for Industry and Research. A DESY / Helmholtz activity
- Download: Pinout for JTAG Switch Module

**Company presentations**
Elma, 14.2.2013

- CERN_ATCA_Presentation_130214.ppt:
- CERN_MicroTCA_System_architecture_1302014.ppt:
- CERN_MTCA_presentation.ppt:

XTCA Web Utilities

- advanced search
- WebTopicList - all topics in alphabetical order
- WebChanges - recent topic changes in this web
- WebNotify - subscribe to an e-mail alert sent when topics change
- WebRss, WebAtom - RSS and ATOM news feeds of topic changes
- WebStatistics - listing popular topics and top contributors
- WebPreferences - preferences of this web

This topic: XTCA > WebHome
Topic revision: r86 - 2022-02-22 - MarkusJoos