

### Frame1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Field		
0	<b>Idle sequence</b>																<b>Frame sync</b>		
1	<b>Idle sequence</b>																		
2	H1	H2	H3	H4													L0Event number		Global Identification
3	-																L0_B_Id		
4	BCSU PT1						BCSU PT2												
5	BCSU Address candidate 1																BCSU Outputs		
6	BCSU Address candidate 2																		
7	F1	F2	F3	F4	PU#1 <sup>st</sup>	PU#2 <sup>nd</sup>	BCSU Status					BCSU BCId							
8	PU0 PT1						PU0 PT2												
9	PU0 Address candidate 1																BCSU Inputs		
10	PU0 Address candidate 2																		
11	-						PU0 Status					PU0 BCId							
12	PU1 PT1						PU1 PT2												
13	PU1 Address candidate 1																		
14	PU1 Address candidate 2																		
15	-						PU1 Status					PU1 BCId							
16	PU2 PT1						PU2 PT2												
17	PU2 Address candidate 1																		
18	PU2 Address candidate 2																		
19	-						PU2 Status					PU2 BCId							
20	PU3 PT1						PU3 PT2												
21	PU3 Address candidate 1																		
22	PU3 Address candidate 2																		
23	-						PU3 Status					PU3 BCId							
24	PU0 Inputs bits 463 to 0 (see format next table)																PU0 Inputs		
25																			
26																			
27																			
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30																			
31																			
32																			
33																			
34																			
35																			
36																			
37																			
38	PU1 inputs bits 463 to 160 (see format next table)																PU1 Inputs		
39																			
40																			
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49																			
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52																			
53	PU1 inputs bits 463 to 160 (see format next table)																PU1 Inputs		
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Frame2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Field
0	idle sequence																Frame sync
1	idle sequence																
2	-	L0Event number															Global Identification
3	-	L0_B_Id															
4	PU2input bits 159 to 0 (see format next table) -																PU1 inputs
5																	
6																	
7																	
8																	
9																	
10																	
11																	
12	PU2Inputs bits 463 to 0 (see format next table) -																PU2 Inputs
13																	
14																	
15																	
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22																	
23																	
24																	
25																	
26																	
27																	
28																	
29																	
30	PU3 Inputs bits 463 to 0 (see format next table)																PU3 Inputs
31																	
32																	
33																	
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36																	
37																	
38																	
39																	
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71																	

PUfield

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	F	
0	-							Optical links error flags									Sign	
1	-	Serial neighbours error flags						Parallel neighbours error flags										
2	M1 optical Inputs																	Optical
3																		
4																		
5																		
6																		
7	M2 optical Inputs																	Optical
8	M3 optical Inputs																	
9	M4 optical inputs																	
10	M5 optical inputs																	
11	M5 optical inputs																	
12	1st backplane serial bus																	Neig transfe (
13	2nd backplane serial bus																	
14	3rd backplane serial bus																	
15	4th backplane serial bus																	
16	5th backplane serial bus																	
17	6th backplane serial bus																	
18	5th backplane serial bus																	Neig transfe I
19	6th backplane serial bus				5th bp //			4th bp //			3rd bp //			2nd bp //				
20	1st bp //		Crossing vertical bus													Neig transfe I		
21	Horizontal parallel bus																	
22																		
23																		
24																		
25	Vertical parallel bus																	
26																		
27																		
28																		-

PUfield

Field
alization
links inputs
ghbours rred at 1.6 Gb/s
ghbours rred at 80 MHz