The Level 0 Pixel Trigger System for the ALICE experiment

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On behalf of the SPD project in the ALICE collaboration

1. Introduction
2. Specifications and constraints
3. System design
4. Development and testing
5. Status of the project

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The ALICE experiment

- **Nucleus-nucleus** collisions at the LHC collider: quark-gluon plasma
- Research program on **p-p interactions**
- **Silicon Pixel Detector (SPD)**
Silicon Pixel Detector

- 120 half staves
  - 2 sensors (160x256 pixels of 425x50 µm²)
  - 10 readout Pixel chips (32x256=8192 channels)
  - 1 on detector readout Multi Chip Module
  - 1 data output 800 Mb/s 1310 nm digital optical link (G-Link)

More details: oral presentation by M. Krivda, “Alice SPD readout electronics”, this conference, this session
Fast-OR

- Fast-OR signals
  - At least 1 pixel hit out of 8192 in a readout chip
  - 1200 Fast-OR signals, 10 on each of 120 data links
  - Low granularity: 1200 equivalent pixels with the size of a chip (~13x13 mm$^2$, pad detector)
  - Transmitted *continuously* every 100 ns

Silicon Pixel Detector
SPD Fast-OR Trigger

- Use the **low granularity** (chip level) Fast-OR information as input to the Central Trigger Processor for Level 0 decision
  - Centrality trigger and selection of impact parameter in heavy ions collisions)

- Different algorithms proposed (topology and multiplicity)
  - GLOBAL OR
  - LAYER
  - SECTOR
  - HALF SECTOR
  - SLIDING WINDOW
  - VERTEX
  - OCCUPANCY

- Combinational functions of **1200 Fast-OR bits**
- Implementation in **large FPGA**
Requirements

• Requirements
  – **Extract** the 1200 Fast-Or signals from the 120 optical data links
  – **Process** them
  – **Generate output** for the Central Trigger Processor
  – Support of **various trigger algorithms** on the **same hardware**
  – User definable trigger algorithms and **remote configuration and control** (control room)

• Constraints
  – Overall process latency: **800 ns**
    (ALICE TDR 010 CERN-LHCC-2003-062)
  – **No interference** on the existing data readout chain
  – System location and space occupation
What do we need to build?

Pixel Trigger System

Optical splitters

Fast-OR extraction

Processing

To DAQ in control room

120 G-Link

1200 bits @ 10 MHz

120 G-Link

Input bandwidth: $120 \cdot 0.8 \text{ Gb/s} = 96 \text{ Gb/s}$

$(120 \cdot 1.6 \text{ Gb/s}) = 192 \text{ Gb/s}$

Output bandwidth: 10 Mb/s
System architecture

Large number of simultaneous inputs to the processing FPGA

High degree of parallelism: latency constraint

Processing time: < 15 ns

Limiting factor: data deserialization and extraction
Optical receiver modules

- **Compact** multi channel optical receiver modules @ 1310 nm *were not found* off the shelf
- **Zarlink** provided two prototypes of *12 inputs* optical fiber receiver modules operating @ 1310 nm
- Significant space saving can be achieved with respect to Small Form Factor standard receivers

![Optical receiver module with 12 optical fiber inputs](image)
Optical receiver modules (qualifying)

- Experimentally qualified
  - Sensitivity
  - Bandwidth (exceeds requirements)
  - Word Error Rate
- The samples fully satisfied the requirements
- A set of customized receivers has been ordered

\[ \Delta t_{\text{rms}} \approx 30 \text{ ps} \]
G-Link deserializers

- **Fast-OR bits** are the payload of the G-Link serial link control words
  - Deserialization and frame alignment
- Three solutions:
  - **Altera** Stratix GX
  - **Xilinx** Virtex 2 Rocket I/O
  - **Dedicated ASIC** (Agilent HDMP1034)

- Tested:
  - **Altera Stratix GX** G-Link deserializer (hardware test)
  - **Virtex 2 Rocket I/O** deserializer (simulation)

### Latency [ns]

<table>
<thead>
<tr>
<th>Device</th>
<th>Data sheet</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Agilent HDMP 1034</td>
<td>88</td>
<td>n.a.</td>
<td>87±7</td>
</tr>
<tr>
<td>Altera Stratix (ver1)</td>
<td>n.a.</td>
<td>190</td>
<td>190</td>
</tr>
<tr>
<td>Altera Stratix (ver2)</td>
<td>n.a.</td>
<td>130</td>
<td>n.a.</td>
</tr>
<tr>
<td>Virtex II Rocket IO X</td>
<td>475</td>
<td>475</td>
<td>n.a.</td>
</tr>
</tbody>
</table>

**Realignment and 8B/10B decoding blocks cannot be bypassed!!**
Optical receiver boards - OPTIN

12 optical inputs
1 Zarlink Parallel Fiber Optic Module
12 Agilent HDMP 1034 G-Link deserializers
1 Xilinx Virtex 4 FPGA (Fast-Or extraction)

Serves two half sectors (6+6 half staves)
  • Extracts 10 Fast-OR bits from each link
  • 120 Fast-OR signals

Dimensions are larger than the IEEE 1386 envelope
12 layers PCB

Almost a Compact PCI card!

Design and layout
PCB prototype production
Installation of components
Testing
Full firmware implementation
Production

26/09/2006

G. Aglieri Rinella, LECC2006, Valencia
Interconnections and routing between OPTIN and BRAIN

- Backplane
- Flat cables
- Daughter cards

Time division multiplexing on 60 lines per OPTIN

Experience with the Router and LinkRx cards of the data readout system (M. Krivda, SPD readout electronics)
Processing Board – BRAIN

9U motherboard

Large I/O space FPGA, 1500 pins

5 OPTIN boards on each side as mezzanine cards

Routing of ~ 1000 lines in the motherboard
  • 800 point to point impedance matched single ended lines
  • Digitally Controlled Impedance

Auxiliary high speed (400 Mbps) optical or LVDS I/O channels

Layout ongoing
Status monitoring and control via Alice Detector Data Link (DDL)
  • Control FPGA
  • Status and control registers in each FPGA

Remote hardware reconfiguration (via DDL) to change the processing algorithm
  • Download firmware in local SRAM memory
  • Program PROMs via JTAG players
  • Launch FPGA reconfiguration

Debugging and local access interfaces (USB, JTAG)

Integration of the system in the Alice Detector Control System
Power dissipation and cooling

High power density

Thermal verification

FEM simulation with dedicated software
  • Three resistors model for each device
  • Board and components thermal conductivity
  • Forced convection
  • Partially enclosed rack

Hot spots in acceptable limits

Courtesy: Emile Dupont
Summary

The ALICE Silicon Pixel Detector 1200 Fast-OR signals will be used to generate an input to the CTP for the Level 0 trigger algorithm.

The ALICE experiment will be the first LHC experiment to include from startup its own silicon vertex detector in the Level 0 decision.

The Alice **Pixel Trigger System is designed and is being constructed**

The Pixel Trigger system:
- targets the stringent **800 ns latency constraint**
- allows for **reconfigurable trigger algorithms**
- is independent from the readout chain
- features a modular and upgradeable design:
  - **OPTIN optical receiver mezzanine boards** with fiber optic receiver modules and G-Link dedicated ASICs
  - **BRAIN Processing board** based on a large logic and I/O space
    - Virtex 4 FPGA
Spares
Acknowledgements: I.A. Cali’, E. P. Dupont, F. Formenti, A. Kluge, M. Krivda, G. Stefanini, F. Vasey, P. Vichoudis,

References:
M. Krivda, “Alice SPD readout electronics”, proceedings of this conference
Signal integrity studies

Signal integrity studies on the communication buses

- **IBIS models** of the Virtex 4 output buffers
- Physical parameters of the board striplines
Radiation effects

Neutron max fluence: $2.0 \cdot 10^8 \text{ cm}^{-2} (10 \text{ y})$


Central Trigger Processor using SRAM based ALTERA Cyclone EP1C20

*Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances, iROC report, 2004*

Failure In Time (FIT): errors in $10^9$ years
SEFI: Single Event Functional Interrupt
SEU: Single Event Upset (configuration)

<table>
<thead>
<tr>
<th></th>
<th>FIT</th>
<th>SEFI</th>
<th>SEU</th>
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<tbody>
<tr>
<td>Altera EP1C20</td>
<td>453</td>
<td></td>
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<tr>
<td>Xilinx XC3S1000</td>
<td>320</td>
<td>1240</td>
<td></td>
</tr>
<tr>
<td>Xilinx XC2V3000</td>
<td>1150</td>
<td>8680</td>
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Errors in 10 years operation

<table>
<thead>
<tr>
<th></th>
<th>SEFI</th>
<th>SEU</th>
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<tbody>
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<td>Altera EP1C20</td>
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<tr>
<td>Xilinx XC3S1000</td>
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<td>18</td>
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<tr>
<td>Xilinx XC2V3000</td>
<td>16</td>
<td>124</td>
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# Trigger latencies and rates

<table>
<thead>
<tr>
<th></th>
<th>Level 0</th>
<th>Level 1</th>
<th>Level 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Last trigger input at CTP (µs)</td>
<td>0.8</td>
<td>6.1</td>
<td>87.6</td>
</tr>
<tr>
<td>Trigger output at CTP (µs)</td>
<td>0.9</td>
<td>6.2</td>
<td>87.7</td>
</tr>
<tr>
<td>Trigger input at detectors (µs)</td>
<td>1.2</td>
<td>6.5</td>
<td></td>
</tr>
<tr>
<td>Rate (Hz)</td>
<td>1000</td>
<td>40-800</td>
<td></td>
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</tbody>
</table>
Time resolution

SPD time resolution: 100 ns
Pileup of event data in p-p interactions at 25 ns bunch crossing rate

clk LHC 40 MHz

clk Pixel 10 MHz

pixel chip

date a

event a/b

event b

date b

pixel trigger

V0

V0 & pixel trigger

event a

event b

A. Kluge