## L0 Trigger Discussion, CERN, 26-June-2014

**Present:**
Richard, Enrico, Massi, Mariana, Plamen, Quentin, Stephane

## ❖ Hardware overview

- The intention is to use a single crate to accommodate the BGV timing and L0 systems
  - A development version of the BGV racks configuration can be found here: `https://twiki.cern.ch/twiki/pub/BGV/CablesAndRacks/RackOrg_v0r6.pdf`
  - **Task1 (Plamen)**: Deliver the TTC crate to P8
    (expect to happen in 1–2 weeks)
- Timing system: RFrx, RF2TTC, Fanout (to be provided by Sophie Baron) and TTCtx (to be provided by Richard)
- L0 system: Logic, Power supply (to be provided by Enrico) and BOBR (available)
- In addition, a VME – USB bridge V1718 (item 0268 in the electronics pool catalog) will be used as a VME system controller (inserted in slot 1)
  - **Task2 (Enrico, Quentin)**: Provide this card
    (relatively urgent)

## ❖ L0 cards

- Logic
  - 4 inputs from the L0 PMTs (2 veto and 2 trigger), discriminators, FPGA
  - 1 ECL output (yes/no) to ODIN
- Power supply
- BOBR
  - 1 TFC fiber as input
  - Distributes the timing over the VME P0 lines to the L0 Logic card
- **Task3 (Richard)**: Confirm with S. Baron that the timing cards are not connected to the P0 bus
- The phase of the BST signal should be monitored (and corrected if needed). A few possibilities were discussed
  1. Standalone L0 monitoring – the bunch slot ID is histogrammed in the L0 Logic FPGA and compared with the expected bunch pattern
  2. Standalone ODIN monitoring – compare the signals from the TFC fiber and ???
  3. Mixed approach – provide a timing signal from the L0 Logic card to ODIN so that it can be compared with ???

## ❖ Control

- PVSS will be used for the control of the L0 system
  - Richard explained that there will be 2 different PVSS projects for the ODIN and the L0 control
- Functional parameters → Translator → HW registers
  - **Task4 (Enrico, Quentin)**: Define the HW registers (addresses, values, etc.) that should be controlled
    - Applies to the Logic, Power supply and BOBR cards
  - **Task5 (Richard)**: Provide the rest (translators, functional parameters, etc.)
- The main L0 configuration will be made with *PVSS recipes*
  - A set of values of the functional parameters
- The development of a PVSS panel would allow to modify specific functional parameters (without creating a new recipe)

## Task List:

**Task1 (Plamen)**: Deliver the TTC crate to P8

**Task2 (Enrico, Quentin)**: Provide this card

**Task3 (Richard)**: Confirm with S. Baron that the timing cards are not connected to the P0 bus

**Task4 (Enrico, Quentin)**: Define the HW registers (addresses, values, etc.) that should be controlled

**Task5 (Richard)**: Provide the rest (translators, functional parameters, etc.)