# Custom V2495 firmware for Bean Monitor System @ CERN

April 26, 2017

The goal of this document is to describe the *Beam Monitor System Custom Firmware for CAEN V2495 module*. It is divided in four section: the first one will describe the principle of work, the second one will describe the internal registers, the third will describe briefly the software functions for delay and parameter settings via VMEbus access and the last one will briefly describe how to install the firmware.

## 1 Principle of Work

The Beam Monitor System at CERN (BMS firmware) is a custom firmware for the CAEN V2495 VME module.

The V2495 module has 32 programmable internal gate and delay generators. Each gate and delay generator is triggered by the rising edge of an internal start signal and it produces a pulse on its output with a programmable delay respect to the start edge and a programmable pulse width (Figure 1).

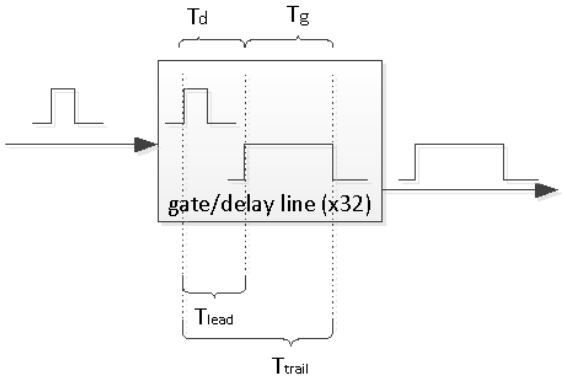


Figure 1: Internal Gate and Delay parameters

The G&D characteristic (dependence of a single cell G&D output delay and width) is illustrated in Figure 2

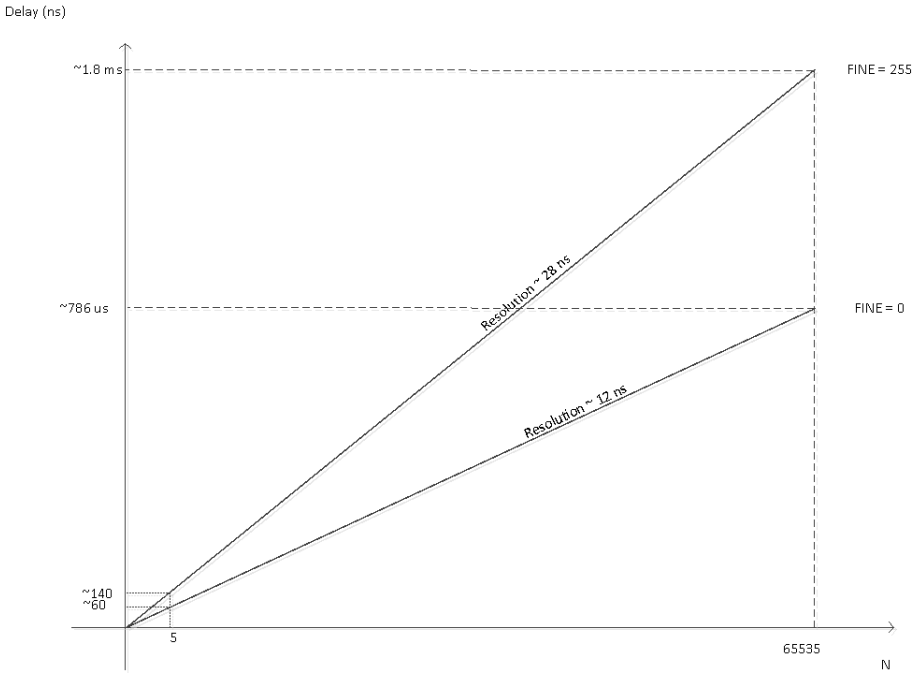


Figure 2: Internal Gate and Delay characteristic

The **N** is a 16-bit parameter (allowed values 0 to 65535). The **Fine** is a 8-bit parameter (allowed values 0 to 255). For each one of the 32 cells available in a V2495 module, the delay value and gate width can be controlled by a separated N parameter (N1 and N2), but their sum cannot exceed 65535. The **Fine** affects **both** the delay and with.

For the scope of this custom firmware, two internal gate and delay generator has been daisy-chaned (Figure 3) in order to have a indipendent setting (for both coarse and fine) for pulse delay (first G&D cell) and pulse width (second G&D cell).

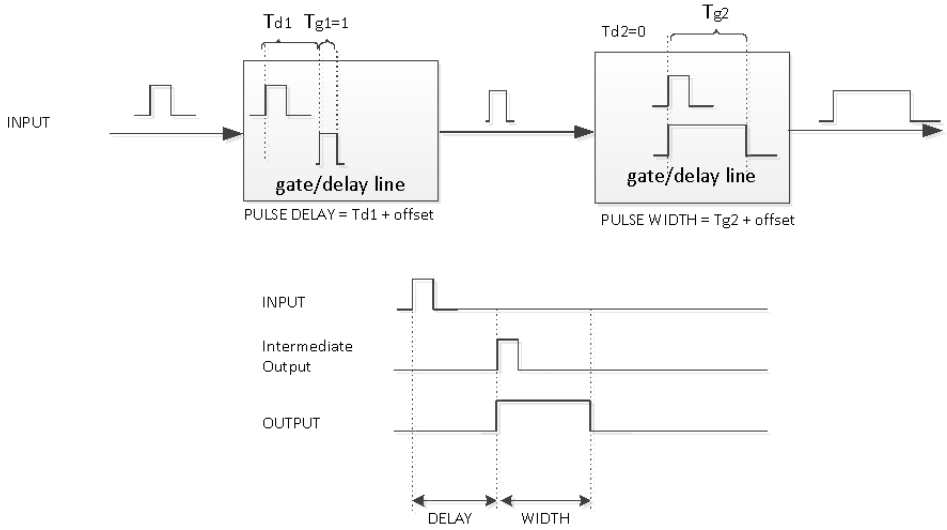


Figure 3: daisy chaining

The firmware accepts 6 ECL inputs signals on A port inputs (A0 to A5). The pulse can be logically inverted. Then the pulse is used to start a corresponding couple of internal gate and delay generator. Each of these internal signal is sent to a A395D mezzanine card installed on port E as monitor.

See Figure 4 for a visual description of the internal firmware implementation.

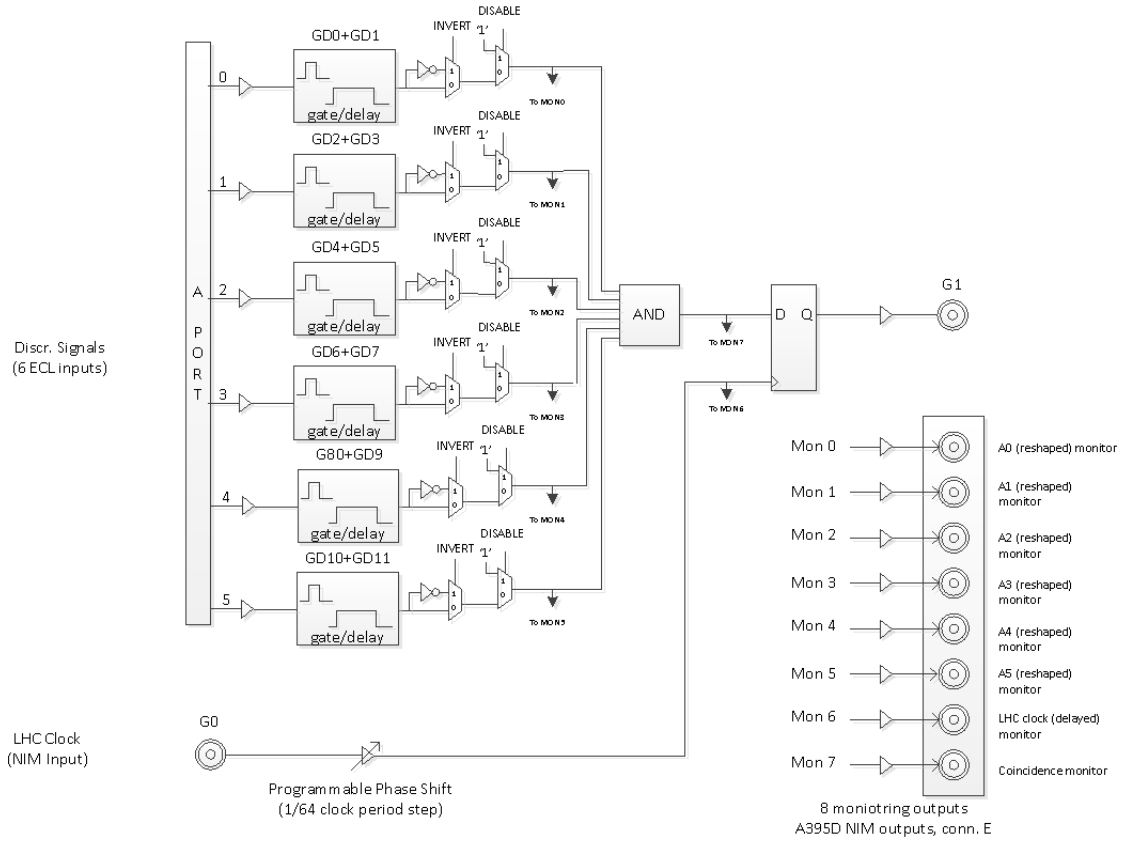


Figure 4: Core logic

Two indipendent internal counters are implemented for test purposes: one is clocked by the internal 50 MHz clock. The other is clocked by the external LHC clock.

The output of one of this counters can be used to trigger a pulse to be generated on the C output port. Each output pulse shape is configured by a couple of internal gate and delay generator channels.

The C ouput can be connected to the A port (input only) via an appropriate adapetr cable (68-pin Robinson-Nugent flat cable).

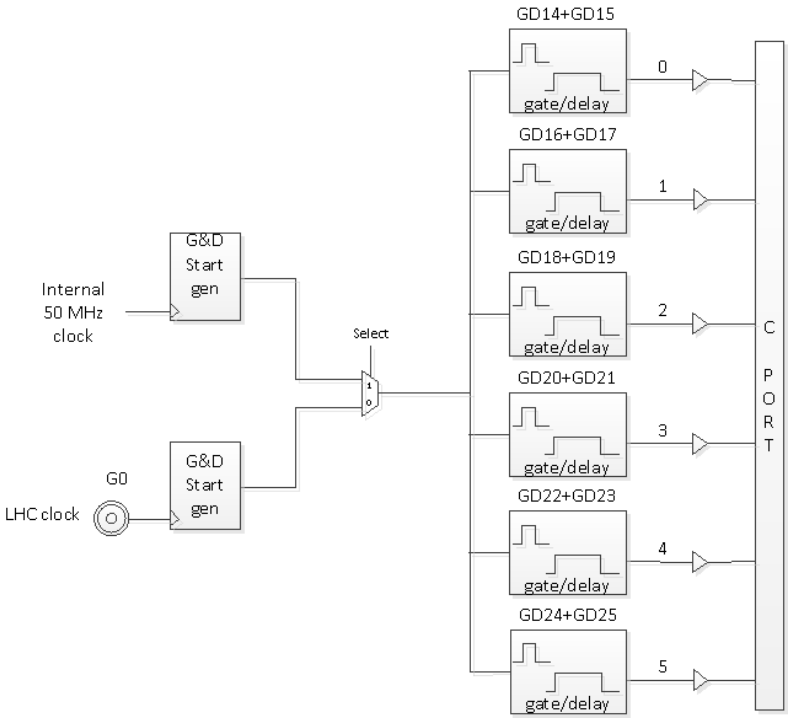


Figure 5: Test generators (drive of C port)

Each input channel can be configured by software through a set of registers

# 2 Registers

The following table describes the registers used to implement the The Beam Monitor System at CERN (BMS firmware).

| Name | Internal Offset | Mode | Description |
|---|---|---|---|
| Firmware revision | 0x1000 | R | Firmware revision id |
| Status register | 0x1004 | R | Contains status informations |
| Input 0 configuration | 0x1800 | R/W | Configure Input 0 mode |
| Input 1 configuration | 0x1804 | R/W | Configure Input 1 mode |
| Input 2 configuration | 0x1808 | R/W | Configure Input 2 mode |
| Input 3 configuration | 0x180C | R/W | Configure Input 3 mode |
| Input 4 configuration | 0x1810 | R/W | Configure Input 4 mode |
| Input 5 configuration | 0x1804 | R/W | Configure Input 5 mode |
| Internal test generator rate | 0x1818 | R/W | Set generator rate |
| Control register | 0x1818 | R/W | Set internal test modes |
| G&D data write register | 0x7f00 | R/W | G&D register (see software functions) |
| G&D command register | 0x7f04 | R/W | G&D register (see software functions) |
| G&D control register | 0x7f08 | R/W | G&D register (see software functions) |
| G&D data read register | 0x7f0C | R/W | G&D register (see software functions) |
| LHC clock phase adjust register | 0x7f20 | R/W | Set LHC clock phase shift |
| LHC clock phase reset register | 0x7f24 | R/W | Reset LHC clock phase shift |

Table 1: Internal registers

## 2.1 Registers description

### 2.1.1 Firmware revision

The initial firmware revision is 1. The firmware revision can be changed by modifying the FWREV constant in the srcV2495_pkg.vhd source file. The firmware must be recompiled and installed.

### 2.1.2 Status register

Bit 0 indicated if the internal PLL locking condition. If it is 0, the external LHC clock connected to G0 input is either unconnected or with a wrong frequency of bad quality. If 1, the LHC clock is connected and with correct parameters.

### 2.1.3 Input Configuration

Each of the six possible inputs has a dedicated register to:

- Invert channel polarity **after** delay (bit0=0 means no inversion; bit0=1 means inversion is enabled)
- Enable channel (bit1 = 0 means enabled (default); bit1 = 1 means channel is disabled)

Only the two less significant bit are used.

### 2.1.4 Internal test generator rate

The internal G&D start generator has a selected rate which can be chosen by using this register. A value of 0 (default) correspond to the maximum possible rate ($Fmax$).

A value of N corresponds to $Fmax/2^N$

### 2.1.5 Control register

A control register is implemented that allows to control some aspect of the board.

| Bit | Name | Description |
|---|---|---|
| 0 | Test source clock | Select internal test generator clock source (0=LHC clock; 1= internal 50 MHz clock) |
| 1 | Monitor configuration | Select Mon 7 monitor output signal (0=Coincidence; 1= LHC clock replica) |
| 2 | NIMTTL | Select if G port is configured as NIM (0) or TTL(1). Default is NIM. |

Table 2: Control register bit map

### 2.1.6 G&D registers

The G&D parameters can be set by a collection of registers. The function of each register is not described here. Please refer to the official CAEN V2495 documentation and above all on the provided C functions.

### 2.1.7 LHC clock phase control registers

The LHC clock phase can be internally shifted by using two registers. The phase adjust register can be used to either increment or decrement the LHC internal delay in 1/64 clock period steps ($1/(40.08 * 64) = 390ps$).

By writing 1 to phase adjust register, the delay is **incremented** by one step. By writing 0 to phase adjust register, the delay is **decremented** by one step.

By writing any value to the phase reset register, the internal LHC clock delay is reset to the initial value.

# 3 Software

The firmware design is accompanied by a set of functions, based on the CAEN CAENComm library.

The functions allow to set the firmware delay parameters as well as to set all configurable parameters.

The list of available functions is declared into the header file gd_func.h in the swlib folder. The function documentation is included prior to every function delaration in the gd_func.h file.

An demo software for parameter setting is provided in the sw/gd_setup folder.

A Visual C++ 2017 solution is provided for compilation (windows platform) of the gd_setup project and gd_test project. The gd_test project is another console application for direct set of a single channel delay parameters.

A Makefile for compoilation of the setup program is provided in the linux folder.

The setup program can be ported to other platforms (not supported by the CAENComm library), by implementig the functions declared in comm.h include file and defined in the comm.c source file.

# 4 Firmware installation

In case of any update to the board firmware, please refer to the V2495 User Manual on the CAEN Website for upgrade instructions.

The file to be used for firmware upgrade is located in fitoutput_files folder and it is named V2495_top.rpd.