

The 742 is a family of 12-bit, 5 GS/s Switched Capacitor Waveform Digitizers based on the DRS4 chip (Paul Scherrer Institute design).

It is available in three form factors: VME (32+2 input channels), NIM (16+1 input channels) and Desktop (16+1 input channels).

Considering the sampling frequency and the bit number, it is well suited for very fast signals as the ones coming from fast scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others.

The analog input signals are continuously sampled into the DRS4 chip in a circular memory buffer (1024 cells) at the default sampling frequency of 5 GS/s (200 ps of sampling period); frequencies of 2.5 or 1 GS/s can also be selected. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits into a digital memory buffer with independent read and write access.

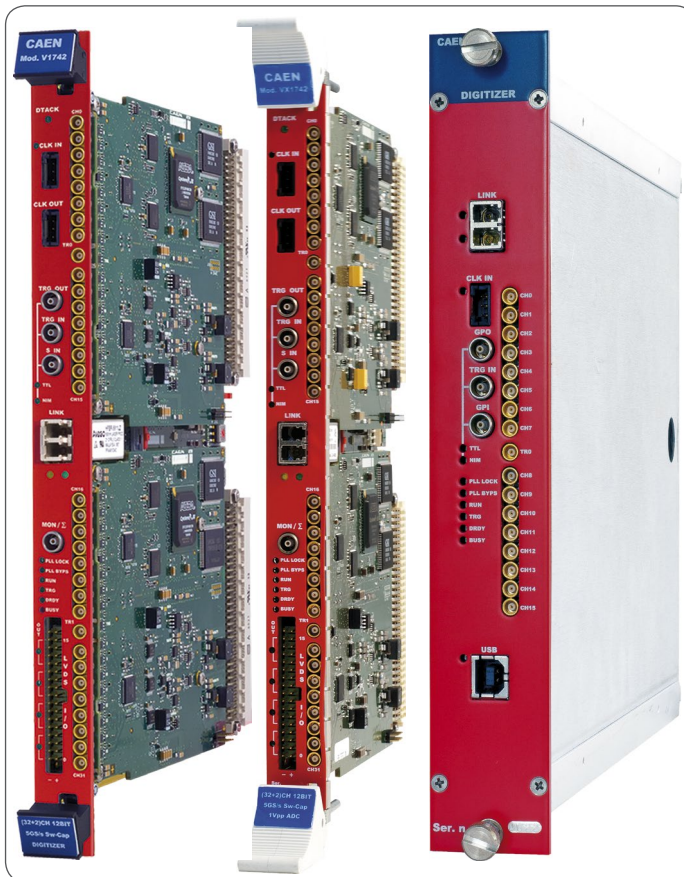
A common acquisition trigger signal can be provided externally via the front panel TRG-IN input as well as via the software but it can also be generated internally thanks to threshold self-trigger capability (only after the A/D conversion, with a trigger latency of 250 ns).

Special analog inputs (TR0 for NIM/Desktop, TR0 and TR1 for VME), can be used as low-latency external trigger signals. These special inputs can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required.

During analog to digital conversion process, the x742 cannot handle other triggers, thus generating a Dead Time.

Two memory sizes are available according to the different versions of the x742 model: 128 or 1024 events, where 1 event is made of 1024 samples.

742 family supports multi-board synchronization allowing all ADCs to be synchronized to a common clock source and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x742 boards.



Highlights

- 12-bit @ 5 GS/s, 1024 samples per event
- 5, 2.5, 1 GS/s software selectable sampling frequencies
- Analog inputs on MCX coax. connectors
- VME64/VME64X (32+2 ch.), NIM (16+1 ch.) and Desktop (16+1 ch.) modules
- 1 Vpp input dynamic range with programmable DC offset adj.
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, C and LabVIEW libraries

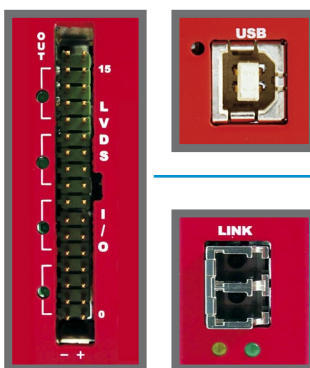
Applications

- Nuclear and Particle Physics
- Astroparticle Physics
- Time of Flight
- Medical Imaging (PET)



x742 is based on the DRS4 a Switched Capacitor Array. This technology relies on a set of capacitors that continuously sample the analog input signals. As soon as the trigger is issued, capacitors are decoupled from the input signals with a time interval from each other that is the sampling period.

The trigger therefore freezes the currently stored signal in the sampling capacitance cells. Subsequently the cells are multiplexed into the 12 bit ADC.



USB

An USB 2.0 link is provided in NIM and Desktop form factors for an easy data readout.

Digital I/O

Digital I/Os are provided in VME boards that can be used for individual trigger propagation to external trigger logic. This feature makes VME form factor ideal to scale up the acquisition channels where a global trigger generation is mandatory.

Optical Link

An Optical link is provided in any form factor for high performance data readout through CAEN proprietary daisy-chainable CONET communication protocol.

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X, 1-unit wide NIM
154x50x164 mm³ (WxHxD) Desktop

ANALOG INPUT

Channels

Single ended, 32+2 ch. (VME), 16+1 ch. (NIM, DESKTOP)

Impedance

50 Ω

Connector

MCX

Full Scale Range (FSR)

1 V_{pp}

Bandwidth

500 MHz

Offset

Programmable DAC for DC offset adjustment per channel or 8-channel group. Range: ±1 V

TR0 TR1 Analog Input

MCX 50 Ω, for fast local trigger and high resolution timing reference. NIM/LVTTL signals also supported.

DIGITAL CONVERSION

Switched Capacitor array

Domino Ring Sampler chip (DRS4), 8+1 channels with 1024 storage cells each

Resolution

12 bits

Sampling rate

1 / 2.5 / 5 GS/s simultaneously on each channel

Dead Time for Event A/D Conversion

110 μs analog inputs only; 181 μs analog inputs + TR0, TR1 inputs

CLOCK GENERATION

Synchronization clock source: internal/external

On-Board PLL provides generation of main board clocks from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

128 event/ch or 1024 event/ch (1024 samples per event) Multi-Event Buffer

TRIGGER

Trigger source

Self-trigger: ch over/under threshold for 16-ch
Common trigger generation (250 ns latency)

Fast local trigger: Programmable threshold on TR0 and TR1 input channels (each TR_n signal triggers two channel groups)

External-trigger: Common by TRG-IN connector

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM and Desktop) output

Trigger Time Stamp

30-bit counter, 8.5 ns resolution (9 s range)

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA
Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM & Desktop direct, VME via V1718 bridge)

USB 2.0 compliant

Transfer rate up to 30 MB/s

VME

VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.7 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 90 mA @ -6 V

VME: 5.5 A @ +5 V, 200 mA @ +12 V, 300 mA @ -12 V

Software

CAEN provides drivers, C and LabVIEW libraries, demo applications and utilities for the complete management of the digitizers, from board configuration to data readout and firmware upgrade.

Windows and Linux 32 and 64 bit operating systems are both supported.



Ordering Code

Code	Description	Form Factor
WDT5742XAAAA	DT5742 - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	Desktop
WDT5742BXAAA	DT5742B - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	Desktop
WN6742XAAAA	N6742 - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	NIM
WN6742BXAAA	N6742B - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	NIM
WV1742XAAAA	V1742 - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	6U-VME64
WV1742BXAAA	V1742B - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	6U-VME64
WVX1742XAAAA	VX1742 - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	6U-VME64X
WVX1742BXAAA	VX1742B - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	6U-VME64X

Accessories

A2818 PCI CONET Controller



A3818 PCI Express CONET2 Controller



A654 MCX to LEMO Cable Adapters



A659 MCX to BNC Cable Adapters



A317 Clock Distribution Cable



A12700 Optical Fiber Series



Cables for CONET Optical Link Networks

