

Technical
Information
Manual

MOD. V 262

*MULTIPURPOSE
I/O REGISTER*

20th January 1992

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Mod V252

DT ACK



OUTECL



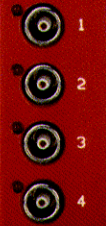
OUT



SHP OUT



IN



cea
I/O REG



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SECTION 1: INTRODUCTION

This module is composed of four different independent subsystems which allow:

- the reading of 4 NIM levels on coaxial inputs;
- the generation of 4 NIM pulses on coaxial outputs;
- the generation of 16 ECL levels on multipoint connectors.

It is realised in a standard one unit wide VME module.

1.1 Principal characteristics

Inputs	4 inputs adapted on 50Ω Standard NIM level
Outputs	4 standard NIM levels 4 standard 140 ns NIM pulses Falling time 3.5 ns Rising time 4.5 ns 16 standard ECL levels
Display	ECL and NIM outputs on LED diodes addressing of the module lasting 1 mSec on a red LED diode
VME Interface	VME A24 D16 protocol Base address fixed by 4 internal rotary switches Reading of the NIM levels register Writing of the NIM pulses register Writing of the NIM levels register Writing of the ECL levels register Reading of the module's identifier Reading of manufacturer's number
Connectors	LEMO 00 Coaxial connectors 34 lead flat cable connectors
Power supply	+5V, 1.1A -12V, 0.5A

SECTION 2: GENERAL DESCRIPTION

2.1 Introduction

The IOREG is a module composed of 4 independent sub systems that allow the reading of input signals and the generation of output signals, or to be more precise, from the VME bus it's possible to perform the following operations:

- the reading of 4 NIM level inputs;
- the writing of 4 NIM level outputs;
- the writing of 16 ECL level outputs;
- the writing of 4 NIM pulse outputs.

2.2 Front panel

It conforms to the standard one unit wide VME with double height, on which you can find 16 ECL data outputs, their LED diodes for each level, 8 NIM outputs, their LED diodes for each level, 4 NIM inputs and their LED diodes indicate each level and a red LED DTACK diode indicating the generation of the VME DTACK signal.

2.2.1 Inputs

The 4 NIM data inputs are situated at the bottom of the board on the front panel (they are marked "IN") and numbered from high to low from 1 to 4. They are built up of 4 coaxial LEMO 00 type connectors with an impedance of 50Ω.

2.2.2 Outputs

The 16 differential ECL outputs are situated at the top of the board and are marked on the front panel "OUT ECL", the first and the last signals are marked "1" and "16" respectively. The logic 1 signals are found on the left contacts and the logic 0 signals are found on the right contacts as you look at the front panel following the normal CEI 912. The 4 NIM level outputs are situated under the ECL outputs, they are numbered from high to low and marked "OUT", under these are situated the NIM pulse outputs. They are numbered from high to low and marked "SHP OUT".

2.2.3 Display

At the top of the panel, a red LED diode called DTACK lights up for about 1 millisecond each time the module generates the DTACK signal on the VME bus.

16 LED diodes display the contents of the ECL registers, and 12 LED diodes display the state of the NIM registers.

2.3 Internal organisation

This module is principally realised in TTL "FAST" logic. It is represented in diagram form in figure 1. The single line represents the connections related with the fast electronics whilst the double lines represent those related with the VME access.

2.3.1 NIM/TTL level inputs and transfers

The NIM signals enter on the coaxial LEMO 00 connector and are adapted by an internal 50 Ω resistor.

2.3.2 TTL/ECL level transfer

A TTL/ECL circuit (MC10124) translator delivers the ECL signals on the JM1 connector.

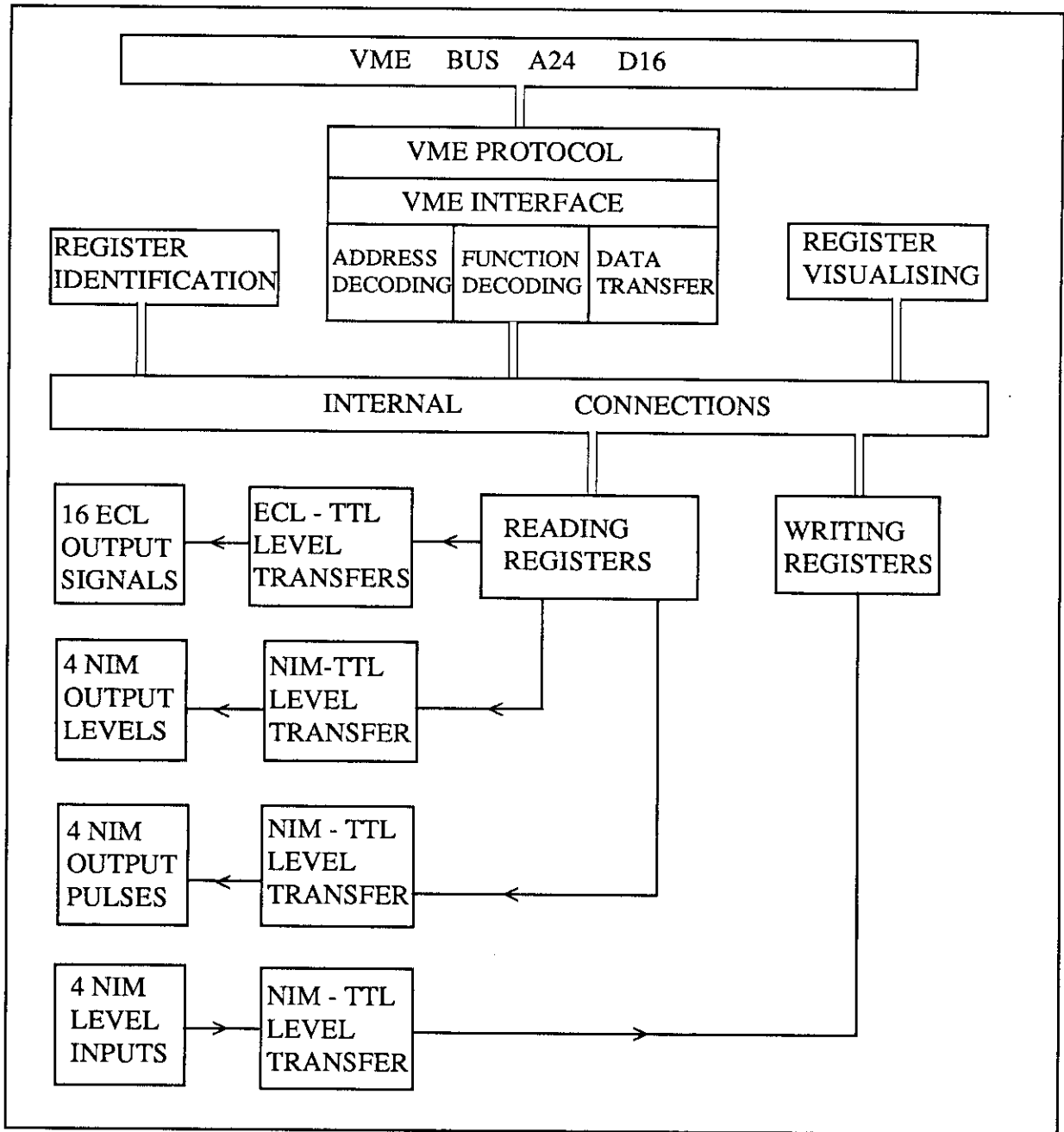


Figure 1 - The principal elements of the IOREG

2.3.3 VME Interface

The module works in A24 D16 mode; this means that the module address must be specified in a field of 24 bits and that the data will be available in words of 16 bits.

The address modifiers used authorise the standard addressing modes in the data space in Supervisor mode or in User mode.

The module's base address is fixed by 4 rotary switches situated on an address decoder sub system (TABOURET VME) fixed on the printed circuit.

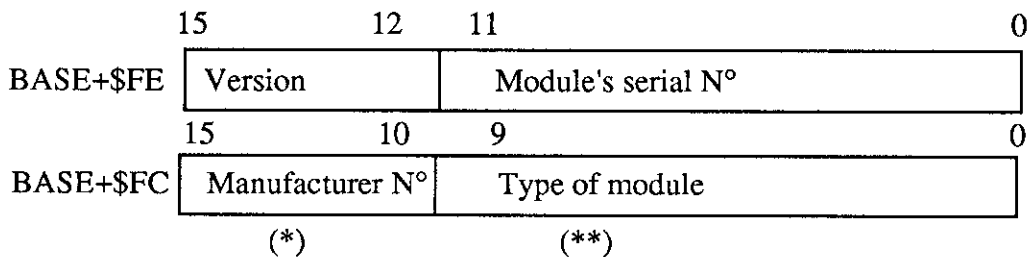
Address in relation to the base address		Installed functions
\$FE	} GR15	Version: D15/D12. Number in the serial type D11/D0
\$FC		
\$FA	} GR14	Construction number: D15/D10, Type: D9/D0
\$FO		
\$EO	} GR13	
\$DO		
\$CO	} GR12	
\$BO		
\$AO	} GR11	
\$90		
\$80	} GR10	
\$70		
\$60	} GR9	
\$50		
\$40	} GR8	
\$30		
\$20	} GR7	
\$10		
\$0A	} GR6	
\$08		
\$06	} GR5	
\$04		
\$00	} GR4	
	} GR3	
	} GR2	
	} GR1	
	} GRO	Reading NIM level
	}	Writing NIM pulse
	}	Writing NIM level
	}	Writing ECL level

Figure 2. I/O Register Address Map

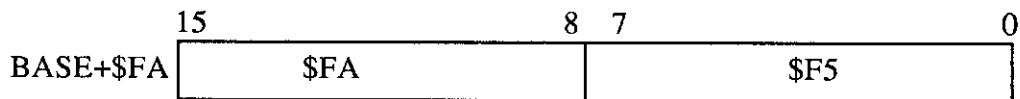
This sub system decodes the 20 most significant bits of the VME address bus, A23 to A4. The 16 bits A23 to A16 are used to define the base address of the module and reserve in this way a page of 256 bytes for each module. The following 4 bits are decoded in a demultiplexer which generates 16 signals defining 16 groups of 16 bytes. The use of the addresses in the module page is represented in figure 2.

A writing cycle to the BASE+\$04 address writes in the ECL level register.
 A writing cycle to the BASE+\$06 address writes in the NIM level register.
 A writing cycle to the BASE+\$08 address writes in the NIM pulse register.
 A reading cycle to the BASE+\$0A address reads in the NIM level register.

The three words, located at the highest address on the page, are used to identify the module as shown in the following tables:



At the BASE+\$FA address two particular bytes are found confirming the presence of the identifier:



The BERR signal (bus error) will be generated for the access at address not used on the page as for all the illegal accesses.

(*) 000010b
 (**) 0000000001b

SECTION 3: UTILISATION

3.1 General Points

Two aspects are to be considered: the fast electronic functions, accessible on the front panel, which perform in real time independently from the VME bus, and the functions connected to the bus.

3.2 How to get started

Before inserting the module into the VME crate you can fix its base address by the rotary switches and verify that it is situated in a free zone of microprocessor memory space. It must be different for each of the modules present in its crate.

Avoid introducing the module when the crate is under voltage.

3.2.1 Input Signals

The 4 NIM standard levels are connected by the coaxial LEMO 00 connector; the inputs are internally adapted.

3.2.2 Output signals

4 standard NIM levels, 4 standard 140 nSec NIM pulses, 16 standard ECL levels.

3.2.3 Data format

The signals present on the inputs 1 to 4 will be related with the bits in positions 1 on 0, 2 on 1, etc. respectively.

3.2.4 Bus role

The VME bus can access the module in two different parts. At the start-up of an acquisition programme, the reading of the identification registers can control the presence of the modules at the foreseen address. This usually serves for program setting.

3.3 Logic

The base address is fixed by the sub-system (VME tabouret) fixed on the board. We read this address in the normal reading way of left to right (see appendix A).

3.3.1 Registers

The VME reading of the NIM levels register at base address+\$0A can be made on a word size.

The VME writing of the NIM pulse register at base address +\$08 can be made on a word size.

The VME writing of the NIM level register at base address +\$06 can be made on a word size.

The VME writing of the ECL level register at base address +\$04 can be made on a word size.

Reading of a module identifier at base address +\$FA can be made by an instruction on a word.

Reading of the manufacturing number at base address +\$FC can be made on a word size.

Reading of the number in the serial type to the base address +\$FE can be made on a word size.

3.3.2 Programming

Example of available programmes. When the base address \$ABCD is in hexadecimals.

DEFINITIONS

NUM.SERIE	EQU	\$ABCD FE
NUM.CONST	EQU	\$ABCDFC
IDENT	EQU	\$ABCDF A
NIVECL	EQU	\$ABCD04
NIVNIM	EQU	\$ABCD06
IMP NIM	EQU	\$ABCD08
ENTNIM	EQU	\$ABCD0A

EXAMPLE 1

Reading the addresses' three highest words on the page in order to read the module identification.

MOVE.W	SERIAL NO., D0
MOVE.W	CONST. NO., D1
MOVE.W	IDENT, D2

EXAMPLE 2

Writing the different values contained in the registers D3, D4, D5

MOVE.W	D3, NIVECL	ACTIVE ECL OUTPUT LEVEL
MOVE.W	D4, NIVNIM	ACTIVE NIM OUTPUT LEVEL
MOVE.W	D5, IMP NIM	ACTIVE NIM OUTPUT PULSE

EXAMPLE 3

Reading the NIM inputs in the D6 register.

MOVE.W	ENTNIM, D6	ACTIVE NIM ENT. INPUTS
--------	------------	------------------------

3.3.3 Initialising

At voltage start up, the contents of the registers do not have any significance.

SECTION 4: DETAILED DESCRIPTION

4.1 Introduction

The module is composed of 4 independent subsystems: 16 differential ECL outputs, 4 NIM level outputs, 4 NIM pulse outputs, 4 NIM level inputs. Each subsystem is composed of two systems: a first circuit system functions under the action of the signals entering and exiting on the front panel. The second system functions under the control of the VME bus, it assures the reading and the writing of the data.

4.1.1 NIM/TTL level inputs and transfers

The NIM input signals enter on the coaxial LEMO 00 connector, 50Ω impedance. The transistors 2N2369 (T1 to T4) mounted on a common base realize the change of NIM/TTL levels transforming the level of current in a voltage limited to the resistance (R15, R17, R19, R21) of its collector; this signal is immediately applied on a Schmitt trigger inverter circuit 74F14 (IC28).

4.1.2 TTL/NIM level outputs and transfers

TTL/NIM level transfer is made in two stages: a change of levels effected by a zener diode (DZ1 to DZ8) 3,3V then a second change of levels with a pair of 2N2369 (T5 to T20), where the transistor is used as current generator. The output signal is available on the transistor collector and exits on a coaxial LEMO 00 connector .

4.1.3 TTL/ECL level outputs and transfers

TTL/ECL level translation is realised in a single step by the intermediary circuits MC10124 (IC2, IC4, IC6, IC7).

4.1.4 Data visualisation

The data visualisation diodes are commanded by the chips 74LS05 (IC5, IC3, IC8, IC21, IC29).

4.1.5 Data memorising

Each datum is memorised by the flip-flop D type (IC9, IC11, IC19, IC23, IC27) where the clock is generated by two pals 22V10 (IC15) which decode the functions used.

4.2 Functions connected to the VME bus

4.2.1 Decoding addresses

The most significant bits of the address (A23 to A4) are decoded in a subsystem (see appendix B) which generates 16 signals (GR1 to GR16) and a valid base address output. The least significant bits (A3, A2, A1) are received by a 74F244 (IC16) and decoded by IC15 (PAL 22V10). The address modifiers, AM5 to AM0 and the internal signals ILWORD and IACK are decoded in the PAL IC17 (16L8 see appendix A) which generates the AMD signal which is sent to the decoding PAL IC15 (22V10). The PAL IC17 also generates the EIDENT signal which allows the reading of the identifier of the module. This signal is sent to the PAL 16L8 (IC13, IC14) which contains the identification words. The internal signals TA1, TA2, TA3, TDS0, TDS1 allow the access to each of the three words located at the following addresses: BASE+\$FA, BASE+\$FC, BASE+\$FC.

4.2.2 Decoding functions

The available functions are decoded in the PAL IC15. To elaborate these signals, the circuit uses the WRITE signals, DS0, DS1 and the signals GR1 and GR15 which comes from the subsystem of address decoding (VME tabouret) and the signal AMD generated by the PAL IC17.

4.2.3 Data Transfer

The different registers communicate with the internal bus through the three state (74F244) (IC16, IC18).

The signals INNIM, ECL, NIV, IMP generated by the PAL IC15 put in service respectively the D type register (74F273), at the time of a VME cycle of writing or reading.

4.3 Protocol Generation

In response to a valid operation, an internal signal IDTACK is generated through a NAND open circuit collector IC20/2 (74F38) which generates the DTACK signal on the VME BUS. The IDTACK signal is connected to a monostable NE555 (IC1), through an inverter 74F04 (IC22/3) which allows the visualisation of this signal DTACK which lasts about 1 millisecond on the red LED diode DTACK situated on the front panel. During an invalid operation, an internal IBERR is generated through a NAND open circuit collector IC20/3 (74F38) which generates BERR on the BUS VME.

4.4 Power Supplies

The IOREG uses the voltages +5V and -12V supplied by the VME bus. The -5V used for the supply of the levels translator is made by an integrated regulator MC7905 (RG1).

APPENDIX A: CHARACTERISTICS OF THE ADDRESS DECODING SUBSYSTEM.

The MSB of the address (A23 to A4) are decoded in this subsystem. The 16 bits A23 to A8 are used to define the base address of the module and reserve in this way a page of 256 bytes for each module. The following 4 bits are decoded in a demultiplexer which generates 16 signals defining internal groups of 16 bytes (GR 0 .. GR 15). The organization of the address decoding subsystem is shown in the following figure.

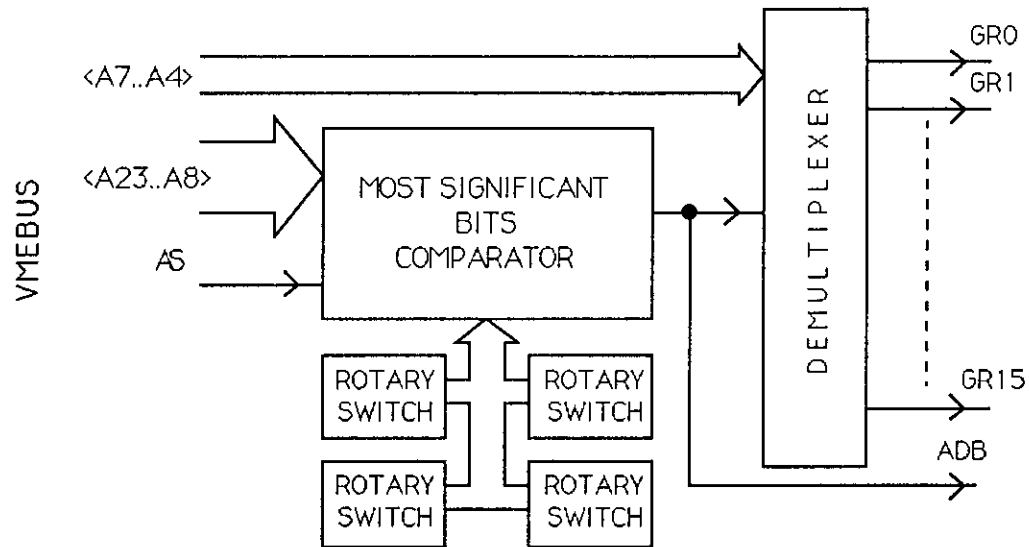


Fig. A.1: Organisation of the address decoding subsystem

The three remaining address bits (A3 to A1), and all the exchange signals with the VMEbus, will be treated in the circuits which are specific for each module.

A.1 Base decoding of the module's address

The decoding of the module's base address is performed by using two comparators 74F521 that compare the value sets on the four hexadecimal rotary switches with the value of the VME address lines A23 to A8. The comparison is enabled by the AS signal to generate the base address signal (ADB). This signal indicates that the module is accessed by VME.

Each rotary switch sets the value of 4 bits of the module's Base address. Figure A.2 on the following page shows the correspondence between the switches and the address bits.

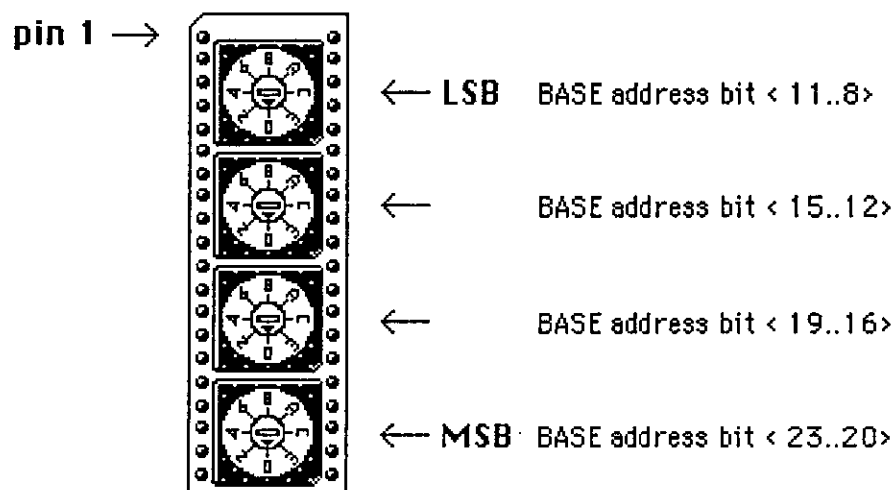


Fig. A.2 : front view of the address decoding subsystem

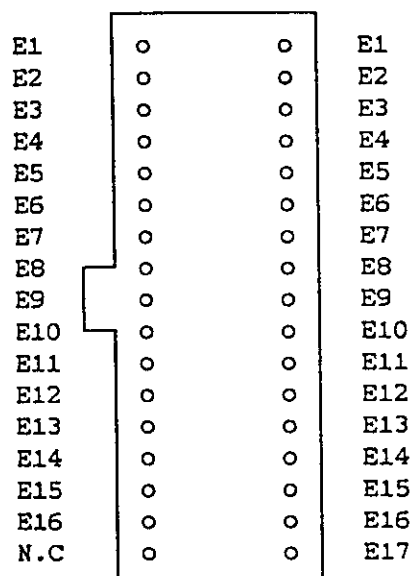
A.2 Decoding of the internal groups

The address lines A7 to A4 are demultiplexed in 16 groups of 16 bytes each, by 2 74LS138 circuits enabled by the base address (ADB). They generate the 16 signals GR0..GR15.

APPENDIX B: CONNECTOR CABLING

B.1 Input connector on the front panel

34 connector contacts seen on the front panel, the contacts are used as follows:



Inputs at "0" -1,7 V -0,9 V

Inputs at "1" -0,9 V -1,7 V