Trigger Logic Board

UniGe GPIO board

Ethernet

CMD Decoder

SW Trigger

Event Buffer

LHC Orbit

BCID Counter

BCR tracker

BCR digitizer

reset

Enable

Event Counter

Deadtime Manager

40 MHz CLK

LHC CLK

LHC Clock

40MHz CLK

veto

Random Trigger

CLK selector

L1A tracker

Delay

L1A - digitizer

Busy Veto

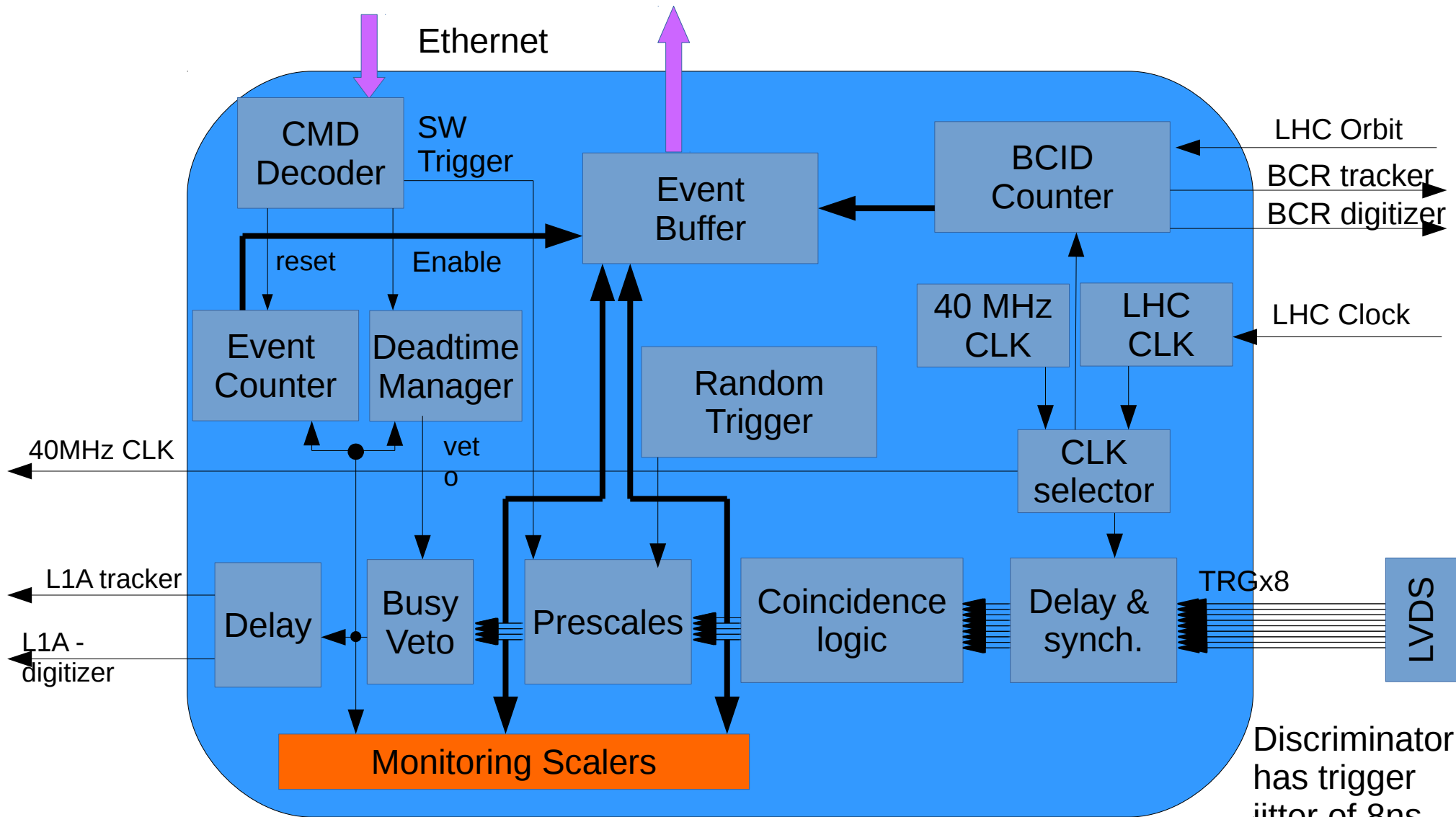Prescales

Coincidence logic

Delay & synch.

TRGx8

LVDS

Monitoring Scalers

Multiple identical outputs
with different delays
for tracker and digitizer

Discriminator
has trigger
jitter of 8ns
Pulse length
set to 32ns