UA43 Dry-Run RAT Réunion Avancement Travaux

HARDWARE COMMISSIONING COORDINATION

26 September 2006 9:00 – CCC

<u>Present</u>: François Chevrier, Robert Harrison, Robin Lauckner, Herve Milcent, Adriaan Rijllart, Antonio Vergara

Progress of the UA43 Dry-Run

- ➢ Report from François and Herve about tests in B1 circuits (600A correctors):
    - o During the PIC1 and PIC2 tests the sequencer access the QPS automatically. However, after each test a human intervention from a QPS expert is needed to reset the system (close the energy extraction switches and go to logging state). This results in a total time testing time per circuit much longer than initially expected.
    - o François thinks that if measures are not taken to speed the process up it will take ages to carry out PIC1 and PIC2 tests. Solutions are:
        - ▪ Automatize reseting of QPS. Allow the sequencer to close the switches and set the QPS in logging mode. François claims that since we are not checking here the QPS behaviour and only the PIC one, the post-mortem analysis of the QPS data could be skipped. Herve says that Reiner do not want anybody, except QPS experts, to carry out such action.
        - ▪ Test the circuits in batteries. This can be done and will be the objective of the tests this week. Nevertheless, some constrains must be taken into account.
    - o Herve explains that only circuits managed by different controllers can be tested in parallel. Currently we have eight B1 and B2 circuits available controlled by two different modules. Circuits will be therefore tested by couples forming 4 different batteries. This should reduce the total test time for the 8 circuits from 80 to 40 minutes.
    - o After the meeting Robin and Herve will list the batteries and at 14:00 the tests will be done. This will be a first test to check whether this grouping of the PIC steps can be extrapolated to a full sector powering test.
- ➢ Adriaan informs that his system is not ready yet to receive real data, trigger the automatic analysis and send the result to the sequencer but the simulator can do the task during these tests.

➤ Antonio reminds that an AUG and UPS failure was expected for this week in order to check the reaction of the software to them. EL is already informed and we can do the test whenever we want. It is decided to postpone such exercise till we have completed the battery tests for B1 and B2.

Open Issues

➤ Controls
  o Some discussions are going on about the alarms. The avalanche of alarms issue must be studied in detail. Robin will follow this up. No news.
➤ QPS
  o Some works at the hardware level still have to be carried out for the 13kA QLC (PCB production). It will be ready by the end of the run. Reiner awaiting reception of software.

Test Schedule

Week 39 (09.25 – 09.29)

- Parallelism and timescales for commissioning
- Battery tests of B1 and B2 circuits.
- PM data analysis (global, connection to sequencer

Week 40 (10.02 – 10.06)

- Validation of PIC1 and PIC2 test procedures as implemented in the sequencer for interface type A with dummy quench loop
- Parallelism and timescales for commissioning including type A
- PM data analysis (global, connection to sequencer)
- PLI and PNO procedures
- Global protection mechanisms (including AUG and UPS fault simulation)
- Others

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Next Dry-Run RAT in CCC: Wednesday 27th at 9:00

Antonio Vergara