UT Inner-backplane Mapping

Zishuo Yang

Aug 3rd, 2017

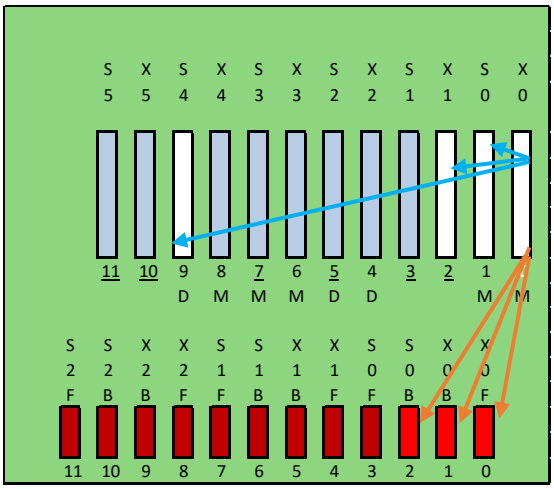
1. Relevant combined-MC/DC-board (**DCB**) slots and Pigtail (**PT**) slots

***Master and SCA are present on the underlined DCBs.**

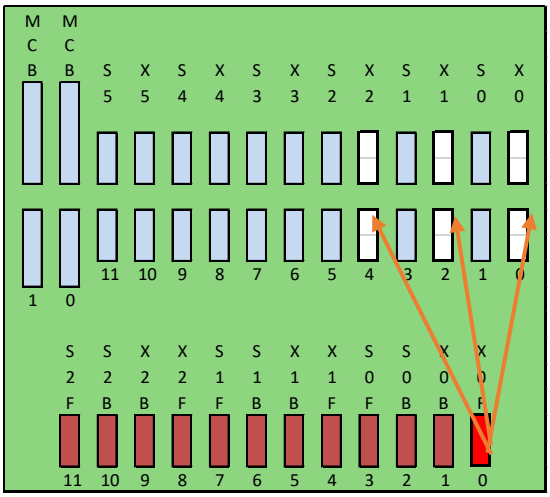
DCB(2,3) are now with GBTx-Tx's. DCB(4,5) are now with Master + SCA. The rest is identical to UT-Middle-backplane.

DCB:	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
PT:	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**

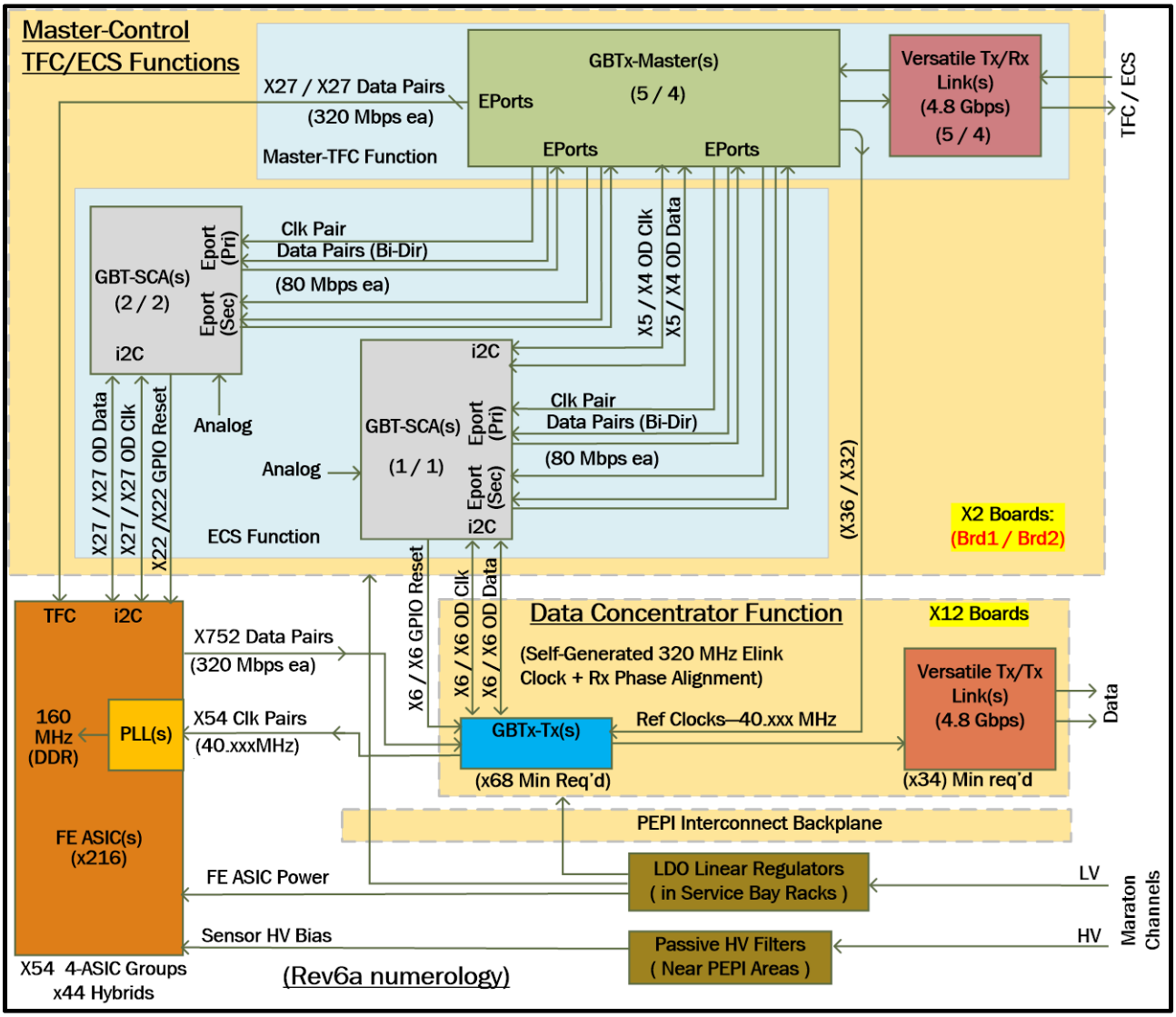
DCB to PT:



PT to DCB:



2. SEAM-pin name definitions



a. ***DC#_ELK***:
Signal Elinks between GBTx-Tx DCs and FE ASICs
b. ***MC_OUT_RCLK***:
Master control reference clock output for DCs
c. ***DC_IN_RCLK***:
Master control reference clock input for DCs
d. ***DC_OUT_RCLK***:
DC reference clock outputs for the Hybrids (always from DC0 on each DCB), from DC to Hybrids (on Pigtail)
e. ***MC_TFC***:
Master control GBTx TFC for hybrids, from Master to Hybrids (on Pigtail)
f. ***MC_SEC***:
Secondary ECS Elink from Master to control of GBT-SCA

g. ***EC_SEC***:
Secondary ECS Elink from SCA to be control by Master
h. ***EC_RESET_GPIO***:
ECS generated reset from SCA to DC and Hybrid. (Also available as general digital I/O)
i. ***DC_RESET***:
Reset common to all DC GBTx's, from SCA to DC
j. ***EC_HYB_i2C***:
ECS generated i2C bus for Hybrids (Data/CLK), from SCA to Hybrids
k. ***DC_i2C***:
ECS i2C bus for DCs, from DC to SCA
l. ***EC_DC_i2C***:
ECS i2C bus for DCs, from SCA to DC
m. ***EC_ADC***:
ADC inputs for ECS SCA, from SCA to DCB and Hybrid thermistors (NOTE: Use AGND as the signal reference.) Reserve _14 and _15 for V rails.
n. ***DC_Thermistor***:
Mounted on DCBs, leg _B connected to AGND
o. ***OM_Thermistor***:
Mounted on Optical Module mezzanine cards, leg _B connected to AGND

3. Mapping design rules

- **DC#_ELK**
  - DCs are assigned according to Jason's ***backplaneMapping_pigtailPins_.xls*** document.
  - Column H assigns a "GBTx ID" to DCs (e.g., 00 – 1 is the 1st DC on DCB 00 / X-0).
  - Columns E and G correspond to the PT slot and pin, mapping DC_ELK_CH to ASIC_CH
  - The order of packing Elinks follows the ***GBTx-DCB Eport Assignment*** as shown below:

6.4 GBTx-DCB Eport Assignments (14 byte data frame using wide-bus mode)

An_x ≡ Asic 'n', byte 'x' where 'x' = 0 ≡ LSB

Group	320 Mb/s GBTx Din Port ID	GBTx Frame Bits	Schematic Mnemonic	3 elink pack (4 ASICs)	4 elink pack (3 ASICs)	5 elink pack (2 ASICs)
5	Dio[5,1]	FRMUP[15:0]	ELK[1:0]	A0_1, A0_2 (MSB)	A0_2, A0_3 (MSB)	A0_3, A0_4 (MSB)
6	Dio[13,9]	FRMUP[31:16]	ELK[3:2]	A1_2 (MSB), A0_0 (LSB)	A0_0 (LSB), A0_1	A0_1, A0_2
0	Din[4,0]	FRMUP[47:32]	ELK[5:4]	A1_0 (LSB), A1_1	A1_2, A1_3 (MSB)	A1_4(MSB), A0_0 (LSB)
1	Din[12,8]	FRMUP[63:48]	ELK[7:6]	A2_1, A2_2 (MSB)	A1_0 (LSB), A1_1	A1_2, A1_3
2	Din[20,16]	FRMUP[79:64]	ELK[9:8]	A3_2 (MSB), A2_0 (LSB)	A2_2, A2_3 (MSB)	A1_0(LSB), A1_1
3	Din[28,24]	FRMUP[95:80]	ELK[11:10]	A3_0 (LSB), A3_1	A2_0 (LSB), A2_1	Fixed Val, Fixed Val
4	Din[36,32]	FRMUP[111:96]	ELK[13:12]	Fixed Val, Fixed Val	Fixed Val, Fixed Val	Fixed Val, Fixed Val

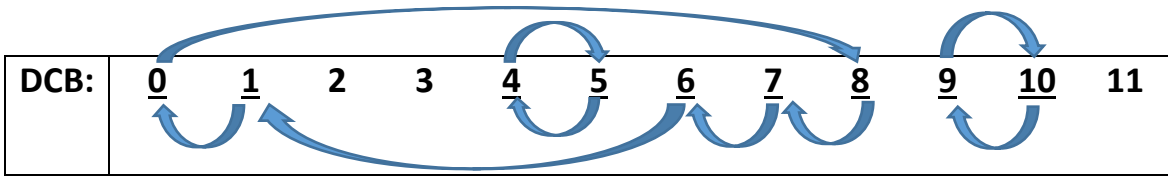
    - The number of elinks per pack is determined by ASIC channels assigned on the corresponding ***backplaneMapping_pigtailPins_.xls*** document.
    - It goes like this (the 4th, the 5th…☺): the first ELK goes with the last channel on the ASIC, second ELK with the second last channel, and so on; Repeat for every ASIC.
  - For unused Elinks due to 5-elink packing, PT pin = "N/A"; PT slot is the same as its siblings'. They are to be tied const to backplane.
  - DCB 2/3 are present in the Inner case, from the blue-traced GBTx DCs on PT(0,1,2,3,4).

- DCB 10/11 were not present in the outer-backplane case, due to the absent outer stave. Correspondingly, PT 8/9/10/11 were not present in the outer-backplane case. For middle-backplane case, these are now added. They are the only difference between UTa-Outer and UT-Middle. DCB(9,10) are now with Master + SCA.

- **MC_OUT_RCLK & DC_IN_RCLK**
  - Ref clocks provided by Master to DCs.
  - Mapping scheme for DCB(0,1,4,5,6,7,8,9) with 5 Masters:
    - Have 8 x 5 = 40 MC_OUT_RCLK, from 5 Masters
    - Need to fill 6 x 8 – (12) = 36 DC_IN_RCLK, from 8 DCBs minus depop'd DCs
    - Ended up using all 40, including 4 depop'd (GBTx ID: 04-5, 05-2, 06-5, 07-2)
  - Mapping scheme for DCB(9,10,11) with 2 Masters:
    - Have 8 x 2 = 16 MC_ from 2 Masters. Need 6x2= 12 DC_ for DCB(10,11); and 2x2 = 4 depop'd on DCB(8,9). Number exactly matched.
  - Mapping scheme for DCB(2,3,4,5) with 2 Masters:
    - Have 16 from 2 Masters. Need 12 for DCB(2,3). The depop'd DCs are all already mapped by the previous 2 schemes (12 DCs in total).

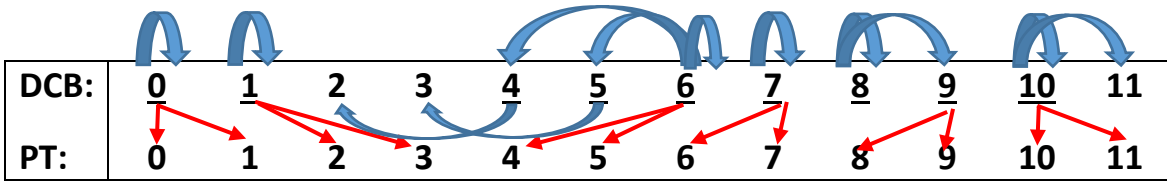
- **MC_TFC**
  - TFC control from Master to Hybrids.
  - Mapping scheme for DCB(0,1,4,5,6,7,8,9) :
    - Have 6 x 5 = 30 MC_TFC. Need 40 – 12 (depop'd) = 28 for Hybrids on PT[00:07] (Inner-backplane Staves B+C). Used 28.
  - Mapping scheme for DCB(9,10,11) :
    - Have 6 x 2 = 12. Need 4+3+3+4 = 14 for Hybrids on PT[08:11].
    - Used all 12, plus 2 previously unused from DCB(8).
  - Mapping scheme for DCB(2,3,4,5) :
    - Have 6 x 2 = 12. Need 12 for depop'd Hybrids. Exactly matched.

- **MC_SEC & EC_SEC**
  - Secondary ECS Elink for Master (MC_SEC) to control SCA (EC_SEC), the SCA being on a different DCB from the Master.
  - Daisy-chain scheme:



- **DC_OUT_RCLK**
  - DC reference clock outputs for the Hybrids, from DCs to Hybrids.
  - Mapping scheme for DCB(0,1,4,5,6,7,8,9) with 5 Masters:
    - Using the DC_OUT_RCLK's from DCBs that have Master/SCA: 8 x 5 = 40 available. Need 40 – 12 (depop'd) = 28 for Hybrids. Used all 40 by including the 12 depop'd.
  - Mapping for DCB(9,10,11) with 2 Masters:
    - Have 8 x 2 = 16 from 2 Masters; need 4 + 3 + 3 + 4 = 14 from PT[8:11]. Used 14.
  - Mapping scheme for DCB(2,3,4,5) :
    - None. All 12 depop'd have been mapped in the previous scheme.

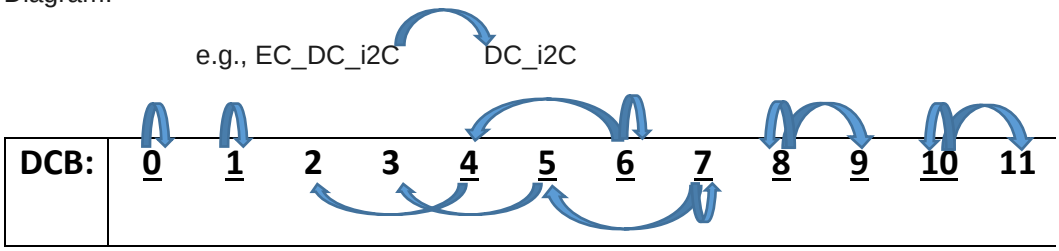
- **EC_RESET_GPIO, DC_RESET, and P#_RESET_P**
  - ECS generated reset from SCA to DC and Hybrid.
  - Mapping scheme for DCB(0,1,4,5,6,7,8,9) with 5 Masters:
    - Have 12 x 5 = 60 EC_RESET's from 5 SCAs
    - Need to be mapped to DC_RESET and P#_RESET_P (positive leg)
    - 8 DC_RESETs from 8 DCBs
    - All P#_RESET_Ps from PT[00:07]. (Including the depop'd since plenty of SCAs)
  - Mapping DCB(9,10,11) with 2 Masters:
    - Have 12 x 2 = 24
    - Need 2 for DC_ on DCB(10,11), and 14 for Hybrids on PT[8:11].
  - Mapping scheme for DCB(2,3,4,5) :
    - Need to map 2 DC_RESETs on DCB(2,3). Used 1 EC_RESET on each DCB(4,5).
  - Diagram: blue is to DCB; red is to Hybrids.



- **EC_HYB_i2C**
  - ECS generated i2C bus for Hybrids (Data/CLK), from SCA to Hybrids.
  - Hybrid channels on PT[00:07] are mapped to SCA channels on DCB(0, 1, 6).
  - PT[08:11] are now fully mapped to DCB(9).

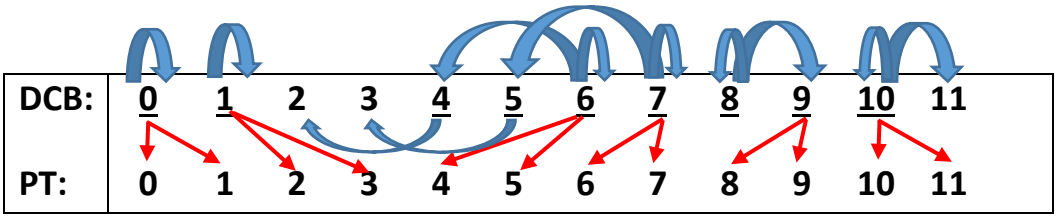
DCB:	0	1	2	3	4	5	6	7	8	9	10	11
PT:	0	1	2	3	4	5	6	7	8	9	10	11

- **DC_i2C & EC_DC_i2C**
  - ECS control i2C bus for DCs, between SCA and DC.
  - 1 DC_i2C per DCB, so 12 DC_i2C.
  - Diagram:



- **EC_ADC, DC_Thermistor, OM_Thermistor**, (and 1V5 / 2V5 in the future)
  - ADC inputs for SCA, from SCA to DCB or Hybrid thermistors (NOTE: Use AGND as the signal reference.) Reserve _14 and _15 for V rails.
  - *Thermistor_B* should always be connected to AGND (analog gnd); so should the PT pins that Nadim named *P#_THERMISTOR_N*.
  - _P should be paired with EC_ADC; _N with AGND. **But not any AGND: only the AGND from the same DCB as the EC_ADC.**
  - We reserve ADC[14:15] on each DCB for V rails (1V5, 2V5).
  - Have 14 x 7 = 98 ADC: from ADC[0:13] on 7 SCAs
  - For DCB(0,1,4,5,6,7,8,9,10,11), need 2 x 10 + 54 = 74.
    - 2 (DC+OM) from each DCB. 40 P#_THERMISTOR_P on PT[00:07];14 on PT[08:11].
  - For DCB(2,3), need 2 x 2 = 4. Used 2 EC_ADC on each DCB(4,5).

- Scheme: (Blue to DCB; red to PT)



- **1V5, 2V5, and GND**
  TBD.

UT Middle-backplane Mapping

Zishuo Yang

July 31, 2017

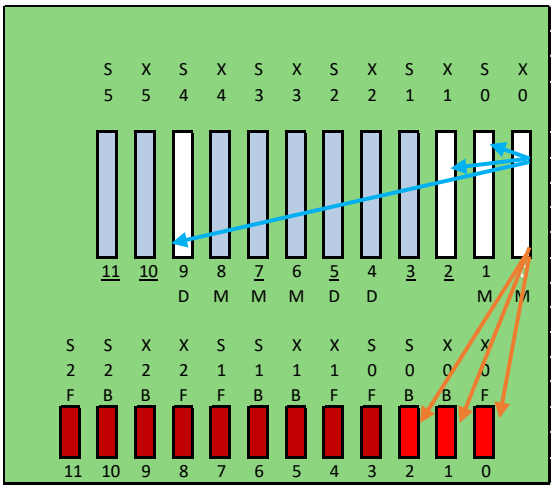
1. Relevant combined-MC/DC-board (**DCB**) slots and Pigtail (**PT**) slots

***Master and SCA are present on the underlined DCBs.**

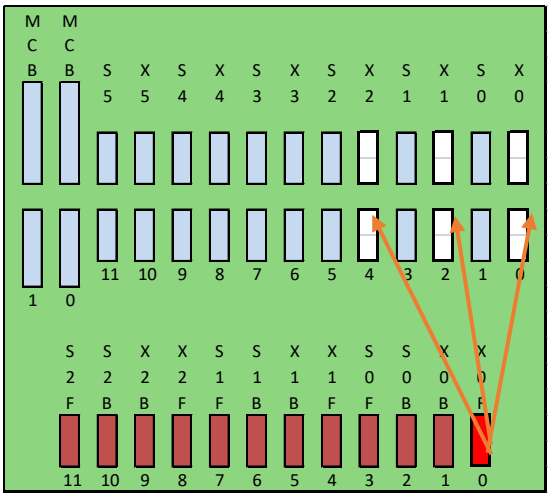
Dark red slots are the added mapping on top of UTa-Outer. The rest is identical to UTa-Outer. DCB(9,10) are now with Master + SCA.

DCB:	**0**	**1**	~~**2**~~	~~**3**~~	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
PT:	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**

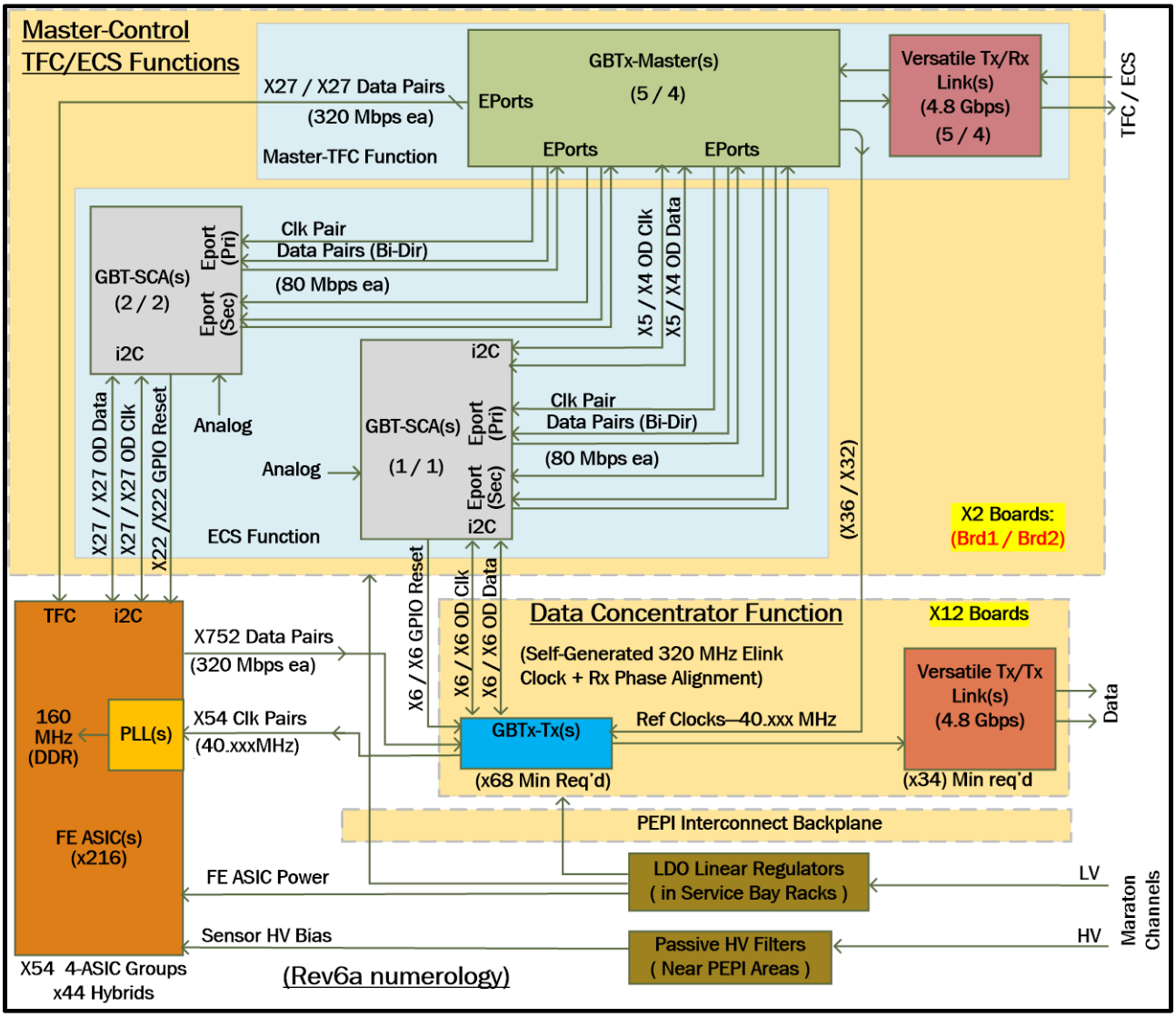
DCB to PT:



PT to DCB:



2. SEAM-pin name definitions



a. ***DC#_ELK***:
Signal Elinks between GBTx-Tx DCs and FE ASICs
b. ***MC_OUT_RCLK***:
Master control reference clock output for DCs
c. ***DC_IN_RCLK***:
Master control reference clock input for DCs
d. ***DC_OUT_RCLK***:
DC reference clock outputs for the Hybrids (always from DC0 on each DCB), from DC to Hybrids (on Pigtail)
e. ***MC_TFC***:
Master control GBTx TFC for hybrids, from Master to Hybrids (on Pigtail)
f. ***MC_SEC***:
Secondary ECS Elink from Master to control of GBT-SCA

g. ***EC_SEC***:
Secondary ECS Elink from SCA to be control by Master
h. ***EC_RESET_GPIO***:
ECS generated reset from SCA to DC and Hybrid. (Also available as general digital I/O)
i. ***DC_RESET***:
Reset common to all DC GBTx's, from SCA to DC
j. ***EC_HYB_i2C***:
ECS generated i2C bus for Hybrids (Data/CLK), from SCA to Hybrids
k. ***DC_i2C***:
ECS i2C bus for DCs, from DC to SCA
l. ***EC_DC_i2C***:
ECS i2C bus for DCs, from SCA to DC
m. ***EC_ADC***:
ADC inputs for ECS SCA, from SCA to DCB and Hybrid thermistors (NOTE: Use AGND as the signal reference.) Reserve _14 and _15 for V rails.
n. ***DC_Thermistor***:
Mounted on DCBs, leg _B connected to AGND
o. ***OM_Thermistor***:
Mounted on Optical Module mezzanine cards, leg _B connected to AGND

3. Mapping design rules

- **DC#_ELK**
  - DCs are assigned according to Jason's ***backplaneMapping_pigtailPins_.xls*** document.
  - Column H assigns a "GBTx ID" to DCs (e.g., 00 – 1 is the 1st DC on DCB 00 / X-0).
  - Columns E and G correspond to the PT slot and pin, mapping DC_ELK_CH to ASIC_CH
  - The order of packing Elinks follows the ***GBTx-DCB Eport Assignment*** as shown below:

6.4 GBTx-DCB Eport Assignments (14 byte data frame using wide-bus mode)

An_x ≡ Asic 'n', byte 'x' where 'x' = 0 ≡ LSB

Group	320 Mb/s GBTx Din Port ID	GBTx Frame Bit	Schematic Mnemonic	3 elink pack (4 ASICs)	4 elink pack (3 ASICs)	5 elink pack (2 ASICs)
5	Dio[5,1]	FRMUP[15:0]	ELK[1:0]	A0_1, A0_2 (MSB)	A0_2, A0_3 (MSB)	A0_3, A0_4 (MSB)
6	Dio[13,9]	FRMUP[31:16]	ELK[3:2]	A1_2 (MSB), A0_0 (LSB)	A0_0 (LSB), A0_1	A0_1, A0_2
0	Din[4,0]	FRMUP[47:32]	ELK[5:4]	A1_0 (LSB), A1_1	A1_2, A1_3 (MSB)	A1_4(MSB), A0_0 (LSB)
1	Din[12,8]	FRMUP[63:48]	ELK[7:6]	A2_1, A2_2 (MSB)	A1_0 (LSB), A1_1	A1_2, A1_3
2	Din[20,16]	FRMUP[79:64]	ELK[9:8]	A3_2 (MSB), A2_0 (LSB)	A2_2, A2_3 (MSB)	A1_0(LSB), A1_1
3	Din[28,24]	FRMUP[95:80]	ELK[11:10]	A3_0 (LSB), A3_1	A2_0 (LSB), A2_1	Fixed Val, Fixed Val
4	Din[36,32]	FRMUP[111:96]	ELK[13:12]	Fixed Val, Fixed Val	Fixed Val, Fixed Val	Fixed Val, Fixed Val

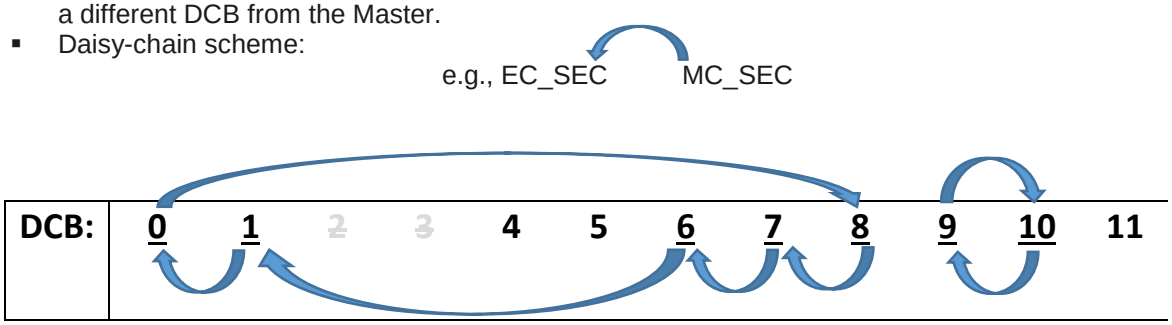
    - The number of elinks per pack is determined by Jason's ***backplaneMapping_pigtailPins_.xls*** document.
    - It goes like this (the 4th, the 5th…☺): the first ELK goes with the last channel on the ASIC, second ELK with the second last channel, and so on; Repeat for every ASIC.
  - For unused Elinks due to 5-elink packing, PT pin = "N/A"; PT slot is the same as its siblings'. They are to be tied const to backplane.
  - DCB 2/3 are depopulated, from the blue-traced GBTx DCs on PT(0,1,2,3,4).

- DCB 10/11 were not present in the outer-backplane case, due to the absent outer stave. Correspondingly, PT 8/9/10/11 were not present in the outer-backplane case. For middle-backplane case, these are now added. They are the only difference between UTa-Outer and UT-Middle. DCB(9,10) are now with Master + SCA.

- **MC_OUT_RCLK & DC_IN_RCLK**
  - Ref clocks provided by Master to DCs.
  - Mapping scheme for 5 Masters on 8 DCBs:
    - Have 8 x 5 = 40 MC_OUT_RCLK, from 5 Masters
    - Need to fill 6 x 8 – (12) = 36 DC_IN_RCLK, from 8 DCBs minus depop'd DCs
    - Ended up using all 40, including 4 depop'd (GBTx ID: 04-5, 05-2, 06-5, 07-2)
  - Mapping scheme for 2 Masters on 3 DCBs:
    - Have 8 x 2 = 16 MC_ from 2 Masters. Need 6x2= 12 DC_ for DCB(10,11); and 2x2 = 4 depop'd on DCB(8,9). Number exactly matched.

- **MC_TFC**
  - TFC control from Master to Hybrids.
  - Mapping scheme for 5 Masters on 8 DCBs:
    - Have 6 x 5 = 30 MC_TFC. Need 40 – 12 (depop'd) = 28 for Hybrids on PT[00:07]. Used 28.
  - Mapping scheme for DCB[9:11]:
    - Have 6 x 2 = 12. Need 4+3+3+4 = 14 for Hybrids on PT[08:11].
    - Used all 12, plus 2 previously unused from DCB(8).

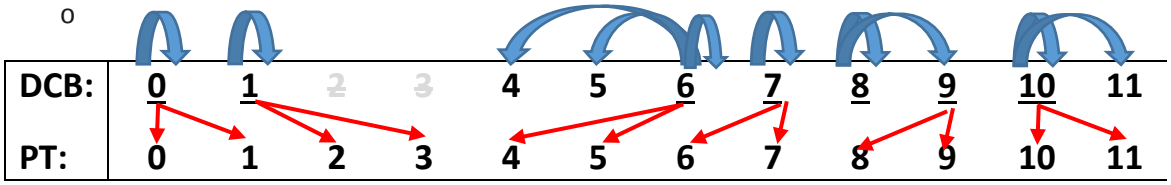
- **MC_SEC & EC_SEC**
  - Secondary ECS Elink for Master (MC_SEC) to control SCA (EC_SEC), the SCA being on a different DCB from the Master.
  - Daisy-chain scheme:



- **DC_OUT_RCLK**
  - DC reference clock outputs for the Hybrids, from DCs to Hybrids.
  - Mapping scheme for 5 Masters on 8 DCBs:
    - Using the DC_OUT_RCLK's from DCBs that have Master/SCA: 8 x 5 = 40 available. Need 40 – 12 (depop'd) = 28 for Hybrids. Used all 40 by including the 12 depop'd.
  - Mapping for DCB[9:11]:
    - Have 8 x 2 = 16 from 2 Masters; need 4 + 3 + 3 + 4 = 14 from PT[8:11]. Used 14.

- **EC_RESET_GPIO, DC_RESET, and P#_RESET_P**
  - ECS generated reset from SCA to DC and Hybrid.
  - Mapping scheme for the 8 DCBs:
    - Have 12 x 5 = 60 EC_RESET's from 5 SCAs
    - Need to be mapped to DC_RESET and P#_RESET_P (positive leg)
    - 8 DC_RESETs from 8 DCBs
    - All P#_RESET_Ps from PT[00:07]. (Including the depop'd since plenty of SCAs)

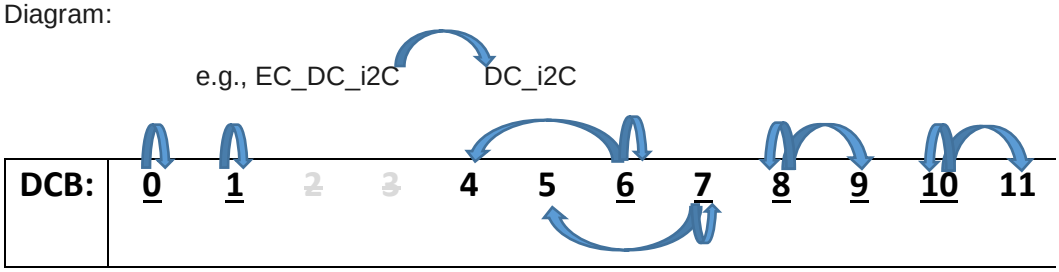
- Mapping DCB[9:11]:
  - Have 12 x 2 = 24
  - Need 2 for DC_ on DCB(10,11), and 14 for Hybrids on PT[8:11].
  - Diagram: blue is to DCB; red is to Hybrids.
  -



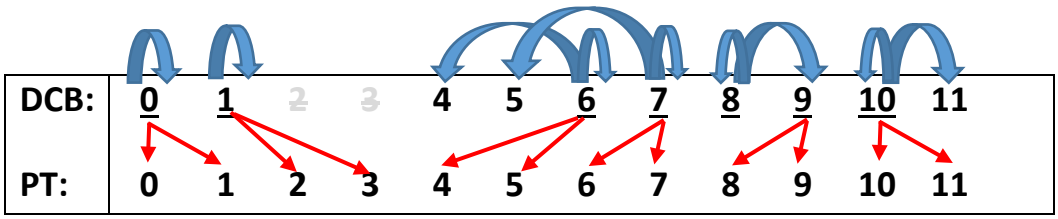
- **EC_HYB_i2C**
  - ECS generated i2C bus for Hybrids (Data/CLK), from SCA to Hybrids.
  - Hybrid channels on PT[00:07] are mapped to SCA channels on DCB(0, 1, 6).
  - PT[08:11] are now fully mapped to DCB(9).

DCB:	0	1	2	3	4	5	6	7	8	9	10	11
PT:	0	1	2	3	4	5	6	7	8	9	10	11

- **DC_i2C & EC_DC_i2C**
  - ECS control i2C bus for DCs, between SCA and DC.
  - 1 DC_i2C per DCB, so 10 DC_i2C.
  - 2 EC_DC_i2C per DCB w/ SCA, so 14 EC_.
  - Diagram:



- **EC_ADC, DC_Thermistor, OM_Thermistor**, (and 1V5 / 2V5 in the future)
  - ADC inputs for SCA, from SCA to DCB or Hybrid thermistors (NOTE: Use AGND as the signal reference.) Reserve _14 and _15 for V rails.
  - *Thermistor_B* should always be connected to AGND (analog gnd); so should the PT pins that Nadim named *P#_THERMISTOR_N*.
  - _P should be paired with EC_ADC; _N with AGND. **But not any AGND: only the AGND from the same DCB as the EC_ADC.**
  - We reserve ADC[14:15] on each DCB for V rails (1V5, 2V5).
  - Have 14 x 7 = 98 ADC: from ADC[0:13] on 7 SCAs
  - Need 2 x 10 + 54 = 74.
    - 2 (DC+OM) from each DCB. 40 P#_THERMISTOR_P on PT[00:07];14 on PT[08:11].
  - Scheme: (Blue to DCB; red to PT)



- **1V5, 2V5, and GND**
  TBD.

UT Detector-plane-a Outer-backplane Mapping

Zishuo Yang

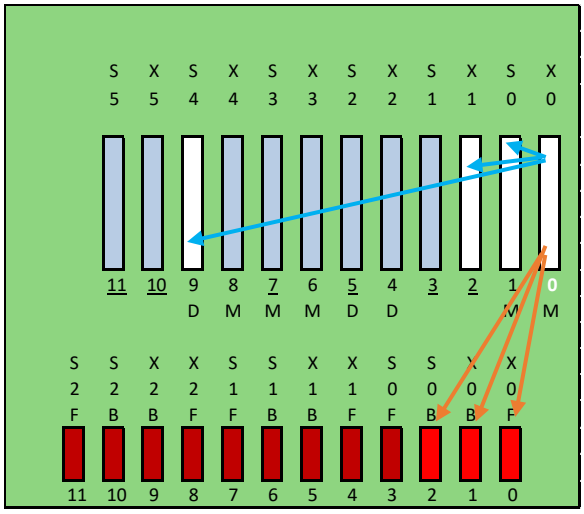
July 25, 2017

1. Relevant combined-MC/DC-board (**DCB**) slots and Pigtail (**PT**) slots

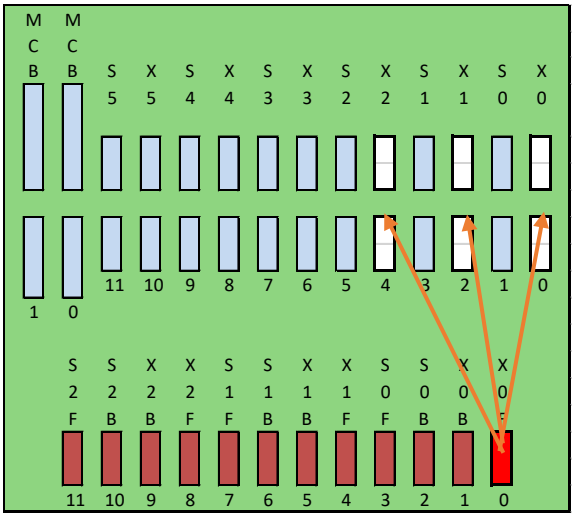
***Master and SCA are present on the underlined DCBs.**

DCB:	**0**	**1**	~~**2**~~	~~**3**~~	**4**	**5**	**6**	**7**	**8**	**9**	~~**10**~~	~~**11**~~
PT:	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	~~**8**~~	~~**9**~~	~~**10**~~	~~**11**~~

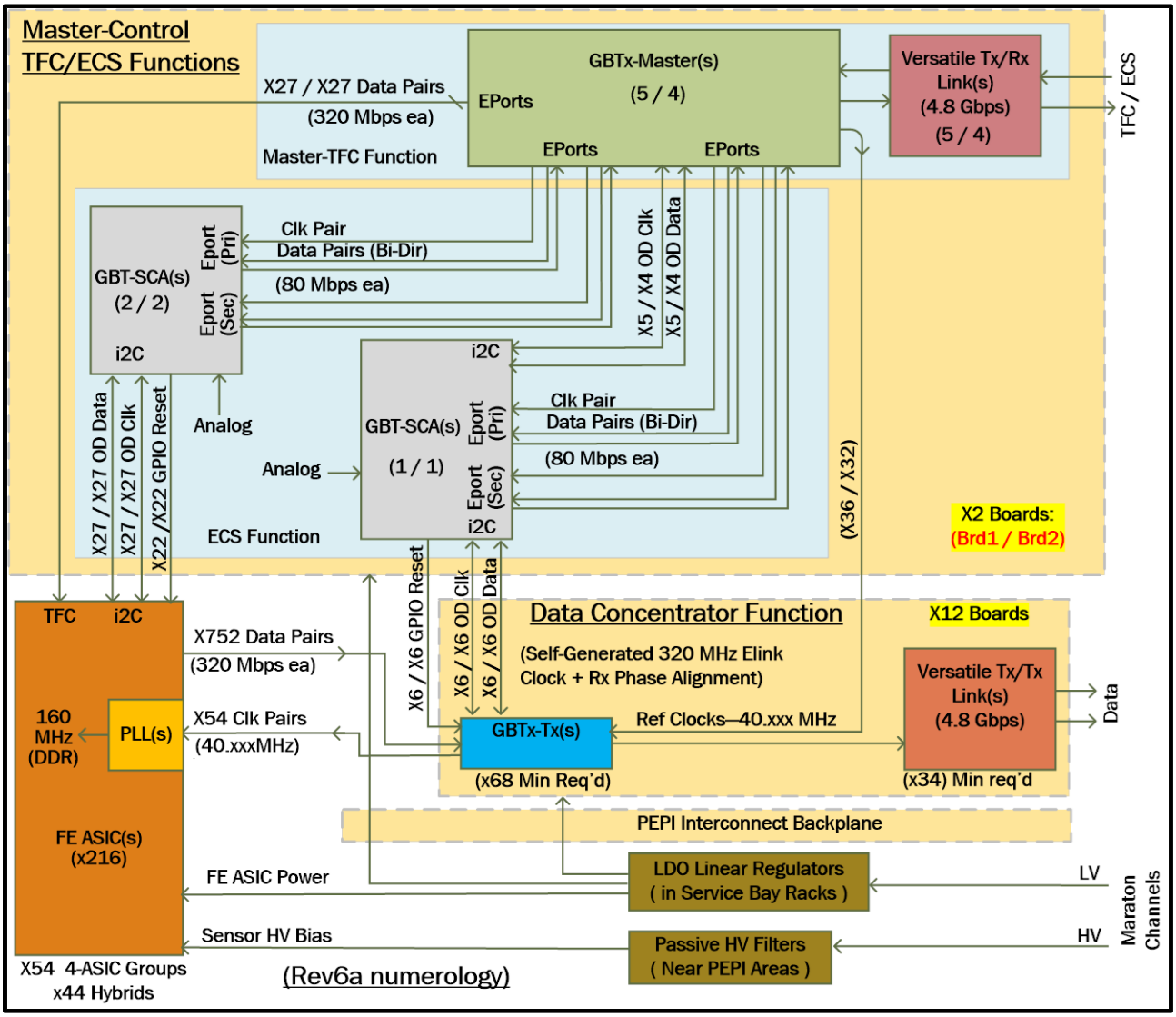
DCB to PT:



PT to DCB:



2. SEAM-pin name definitions



a. ***DC#_ELK***:
Signal Elinks between GBTx-Tx DCs and FE ASICs
b. ***MC_OUT_RCLK***:
Master control reference clock output for DCs
c. ***DC_IN_RCLK***:
Master control reference clock input for DCs
d. ***DC_OUT_RCLK***:
DC reference clock outputs for the Hybrids (always from DC0 on each DCB), from DC to Hybrids (on Pigtail)
e. ***MC_TFC***:
Master control GBTx TFC for hybrids, from Master to Hybrids (on Pigtail)
f. ***MC_SEC***:
Secondary ECS Elink from Master to control of GBT-SCA
g. ***EC_SEC***:
Secondary ECS Elink from SCA to be control by Master

h. ***EC_RESET_GPIO***:
ECS generated reset from SCA to DC and Hybrid. (Also available as general digital I/O)
i. ***DC_RESET***:
Reset common to all DC GBTx's, from SCA to DC
j. ***EC_HYB_i2C***:
ECS generated i2C bus for Hybrids (Data/CLK), from SCA to Hybrids
k. ***DC_i2C***:
ECS i2C bus for DCs, from DC to SCA
l. ***EC_DC_i2C***:
ECS i2C bus for DCs, from SCA to DC
m. ***EC_ADC***:
ADC inputs for ECS SCA, from SCA to DCB and Hybrid thermistors (NOTE: Use AGND as the signal reference.) Reserve _14 and _15 for V rails.
n. ***DC_Thermistor***:
Mounted on DCBs, leg _B connected to AGND
o. ***OM_Thermistor***:
Mounted on Optical Module mezzanine cards, leg _B connected to AGND

3. Mapping design rules

- **DC#_ELK**
  - DCs are assigned according to Jason's ***backplaneMapping_pigtailPins_.xls*** document.
  - Column H assigns a "GBTx ID" to DCs (e.g., 00 – 1 is the 1st DC on DCB 00 / X-0).
  - Columns E and G correspond to the PT slot and pin, mapping DC_ELK_CH to ASIC_CH
  - The order of packing Elinks follows the ***GBTx-DCB Eport Assignment*** as shown below:

6.4 GBTx-DCB Eport Assignments (14 byte data frame using wide-bus mode)

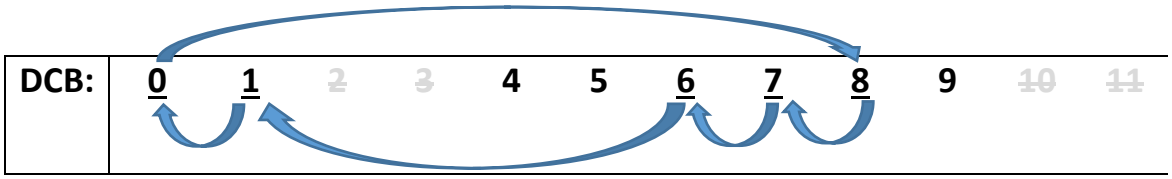
An_x ≡ Asic 'n', byte 'x' where 'x' = 0 ≡ LSB

Group	320 Mb/s GBTx Din Port ID	GBTx Frame Bit	Schematic Mnemonic	3 elink pack (4 ASICs)	4 elink pack (3 ASICs)	5 elink pack (2 ASICs)
5	Dio[5,1]	FRMUP[15:0]	ELK[1:0]	A0_1, A0_2 (MSB)	A0_2, A0_3 (MSB)	A0_3, A0_4 (MSB)
6	Dio[13,9]	FRMUP[31:16]	ELK[3:2]	A1_2 (MSB), A0_0 (LSB)	A0_0 (LSB), A0_1	A0_1, A0_2
0	Din[4,0]	FRMUP[47:32]	ELK[5:4]	A1_0 (LSB), A1_1	A1_2, A1_3 (MSB)	A1_4(MSB), A0_0 (LSB)
1	Din[12,8]	FRMUP[63:48]	ELK[7:6]	A2_1, A2_2 (MSB)	A1_0 (LSB), A1_1	A1_2, A1_3
2	Din[20,16]	FRMUP[79:64]	ELK[9:8]	A3_2 (MSB), A2_0 (LSB)	A2_2, A2_3 (MSB)	A1_0(LSB), A1_1
3	Din[28,24]	FRMUP[95:80]	ELK[11:10]	A3_0 (LSB), A3_1	A2_0 (LSB), A2_1	Fixed Val, Fixed Val
4	Din[36,32]	FRMUP[111:96]	ELK[13:12]	Fixed Val, Fixed Val	Fixed Val, Fixed Val	Fixed Val, Fixed Val

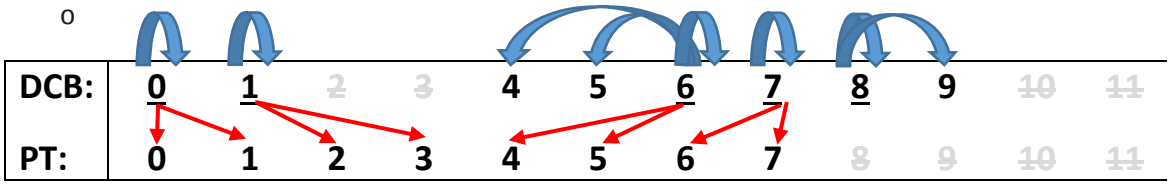
    - The number of elinks per pack is determined by Jason's ***backplaneMapping_pigtailPins_.xls*** document.
    - It goes like this (the 4th, the 5th…☺): the first ELK goes with the last channel on the ASIC, second ELK with the second last channel, and so on; Repeat for every ASIC.
  - For unused Elinks due to 5-elink packing, PT pin = "N/A"; PT slot is the same as its siblings'. They are to be tied const to backplane.
  - DCB 2/3 are depopulated, from the blue-traced GBTx DCs on PT 0/1/2/3.

- DCB 10/11 are not present in the outer-backplane case, due to the absent outer stave. Correspondingly, PT 8/9/10/11 are not present in the outer-backplane case, neither. [TO BE DOUBLE-CHECKED].

- **MC_OUT_RCLK & DC_IN_RCLK**
  - Ref clocks provided by Master to DCs.
  - Mapping scheme for 5 Masters on 8 DCBs:
    - Have 8 x 5 = 40 MC_OUT_RCLK, from 5 Masters
    - Need to fill 6 x 8 – (12) = 36 DC_IN_RCLK, from 8 DCBs minus depop'd DCs
    - Ended up using all 40, including 4 depop'd (GBTx ID: 04-5, 05-2, 06-5, 07-2)
- **MC_TFC**
  - TFC control from Master to Hybrids.
  - Mapping scheme for 5 Masters on 8 DCBs:
    - Have 6 x 5 = 30 MC_TFC
    - Need 40 – 12 (depop'd) = 28 for Hybrids on PT[00:07]
    - Used 28
- **MC_SEC & EC_SEC**
  - Secondary ECS Elink for Master (MC_SEC) to control SCA (EC_SEC), the SCA being on a different DCB from the Master.
  - Daisy-chain scheme:



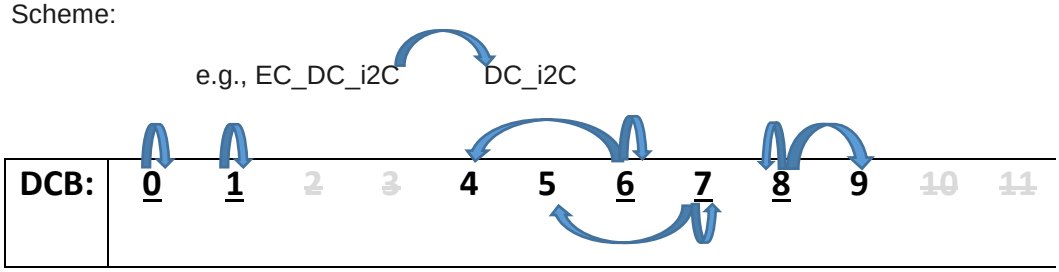
- **DC_OUT_RCLK**
  - DC reference clock outputs for the Hybrids, from DCs to Hybrids.
  - Using the DC_OUT_RCLK's from DCBs that have Master/SCA: 8 x 5 = 40 available
  - Need 40 – 12 (depop'd) = 28 for Hybrids
  - Used all 40 by including the 12 depop'd
- **EC_RESET_GPIO, DC_RESET, and P#_RESET_P**
  - ECS generated reset from SCA to DC and Hybrid.
  - Have 12 x 5 = 60 EC_RESET's from 5 SCAs
  - Need to be mapped to DC_RESET and P#_RESET_P (positive leg)
    - 8 DC_RESETs from 8 DCBs
    - All P#_RESET_Ps from PT[00:07]. (Including the depop'd since plenty of SCAs)
    - Scheme: (Blue is to DCB; Red is to Hybrids)
    -



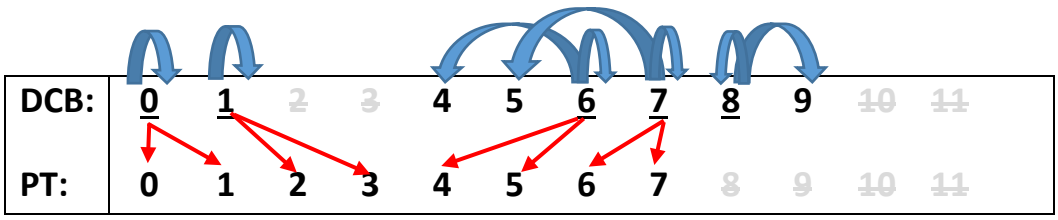
- **EC_HYB_i2C**
  - ECS generated i2C bus for Hybrids (Data/CLK), from SCA to Hybrids.
  - Hybrid channels on PT[00:07] are mapped to SCA channels on DCB(0, 1, 6).
    - For future mapping, PT[08:11] are currently mapped to DCB(9). But this doesn't concern the outer-backplane case.

DCB:	0	1	2	3	4	5	6	7	8	9	10	11
PT:	0	1	2	3	4	5	6	7	8	9	10	11

- **DC_i2C & EC_DC_i2C**
  - ECS control i2C bus for DCs, between SCA and DC.
  - 1 DC_i2C per DCB, so 8; 2 EC_DC_i2C per DCB w/ SCA, so 10.
  - Scheme:



- **EC_ADC, DC_Thermistor, OM_Thermistor**, (and 1V5 / 2V5 in the future)
  - ADC inputs for SCA, from SCA to DCB or Hybrid thermistors (NOTE: Use AGND as the signal reference.) Reserve _14 and _15 for V rails.
  - *Thermistor_B* should always be connected to AGND (analog gnd); so should the PT pins that Nadim named *P#_THERMISTOR_N*.
  - _P should be paired with EC_ADC; _N with AGND. **But not any AGND: only the AGND from the same DCB as the EC_ADC.**
  - We reserve ADC[14:15] on each DCB for V rails (1V5, 2V5).
  - Have 14 x 5 = 70 ADC: from ADC[0:13] on 5 SCAs
  - Need 2 x 8 + 40 = 56.
    - 2 (DC+OM) from each DCB; 40 P#_THERMISTOR_P on PT[00:07]
  - Scheme: (Blue to DCB; red to PT)



- **1V5, 2V5, and GND: TBD**