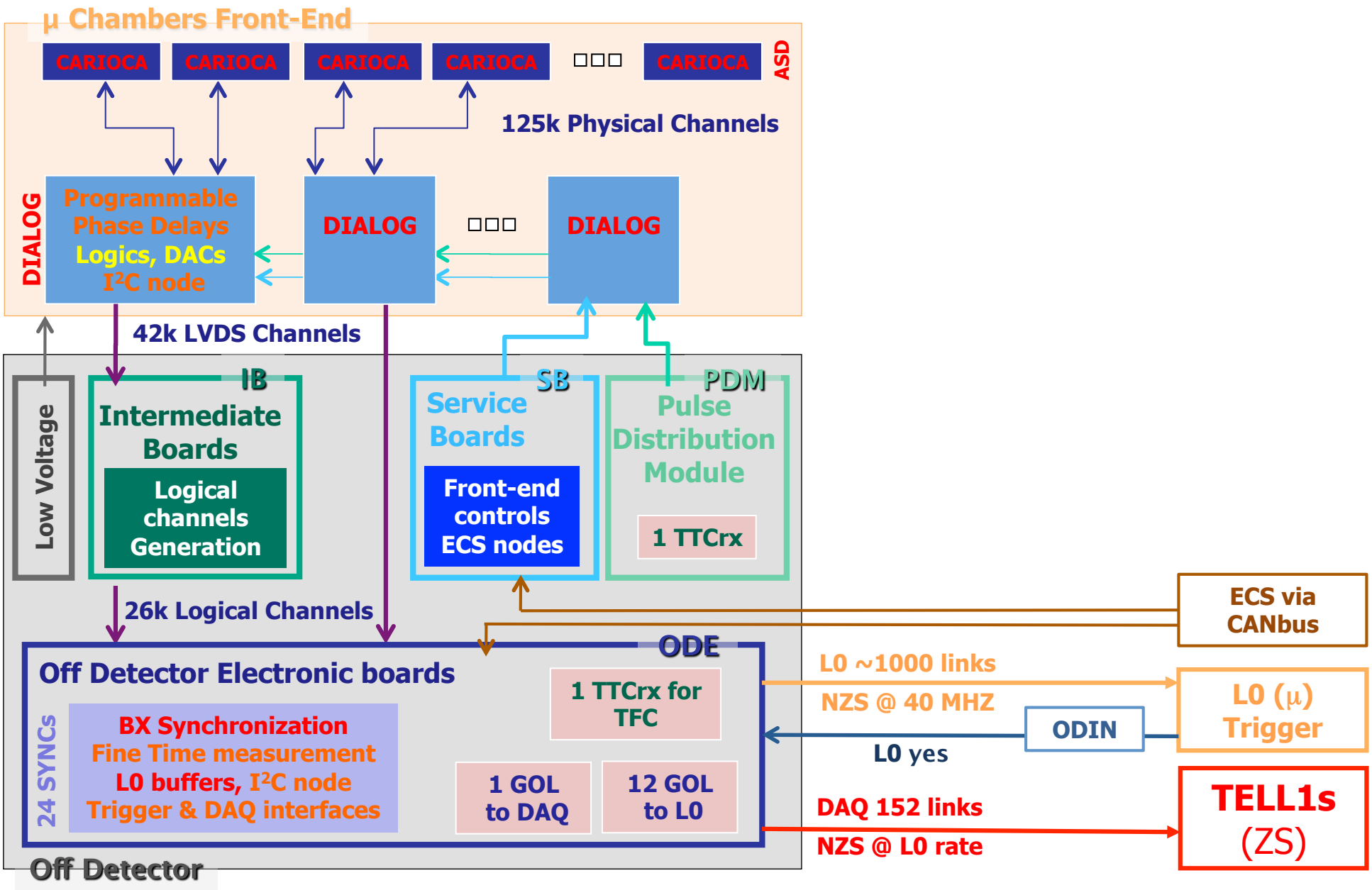
LHCb Upgrade Mini-Workshop on PID

Muon Readout

Outline

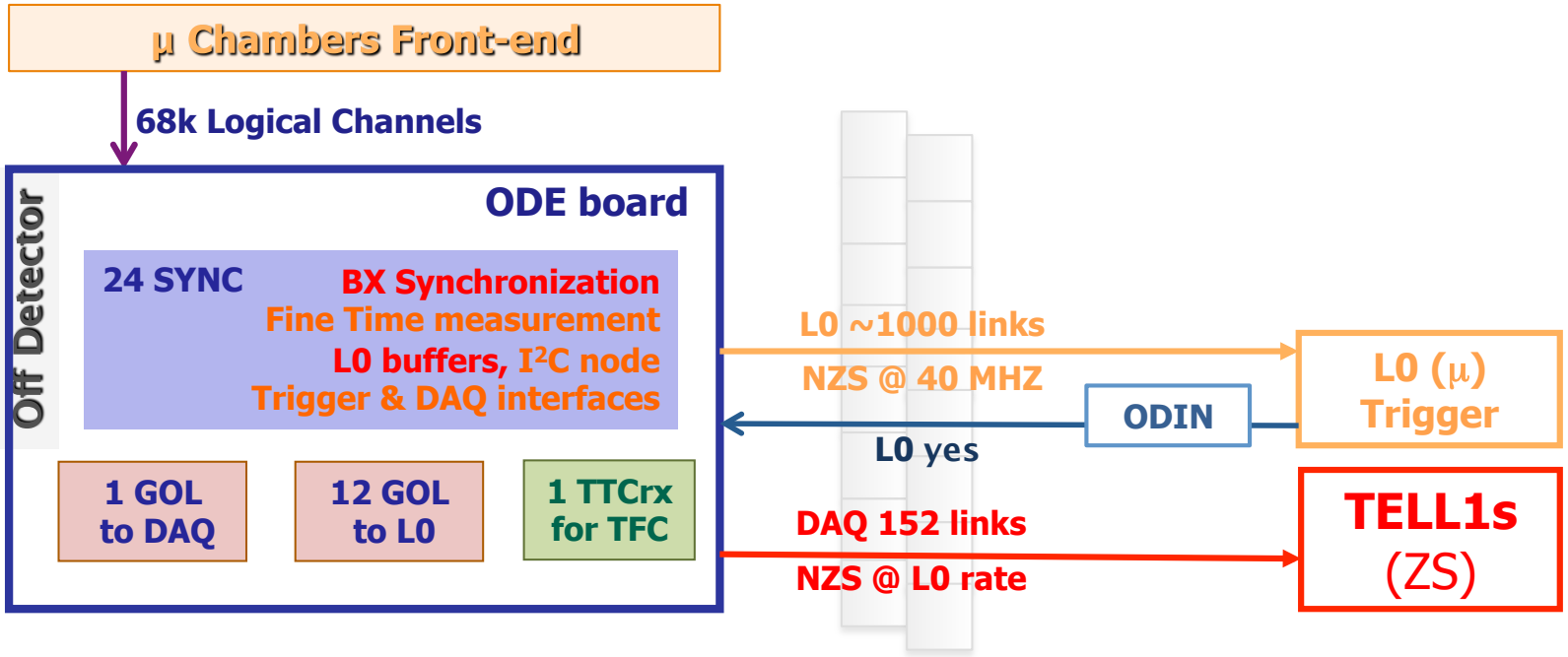
- Electronics architecture for the upgrade
  - Present Architecture
  - What changes for the Upgrade
- Implementation on TELL40
  - In/Out Requirements to fit the existing hardware
  - Dedicated ACQ_Muon Firmware
- Conclusions

Present Muon Electronics Architecture



Present Muon Electronics Architecture

1. 5 μ stations: M1 M2 M3 M4 M5
   → 152 ODE boards (Off Detector Electronics)
2. **L0 link**: hit/channel information @ 40 MHz to L0 mu trigger
3. **DAQ link**: 4 bits TDC information to TELL1 @ max 1 MHz
4. ECS communication via CANbus and ELMB



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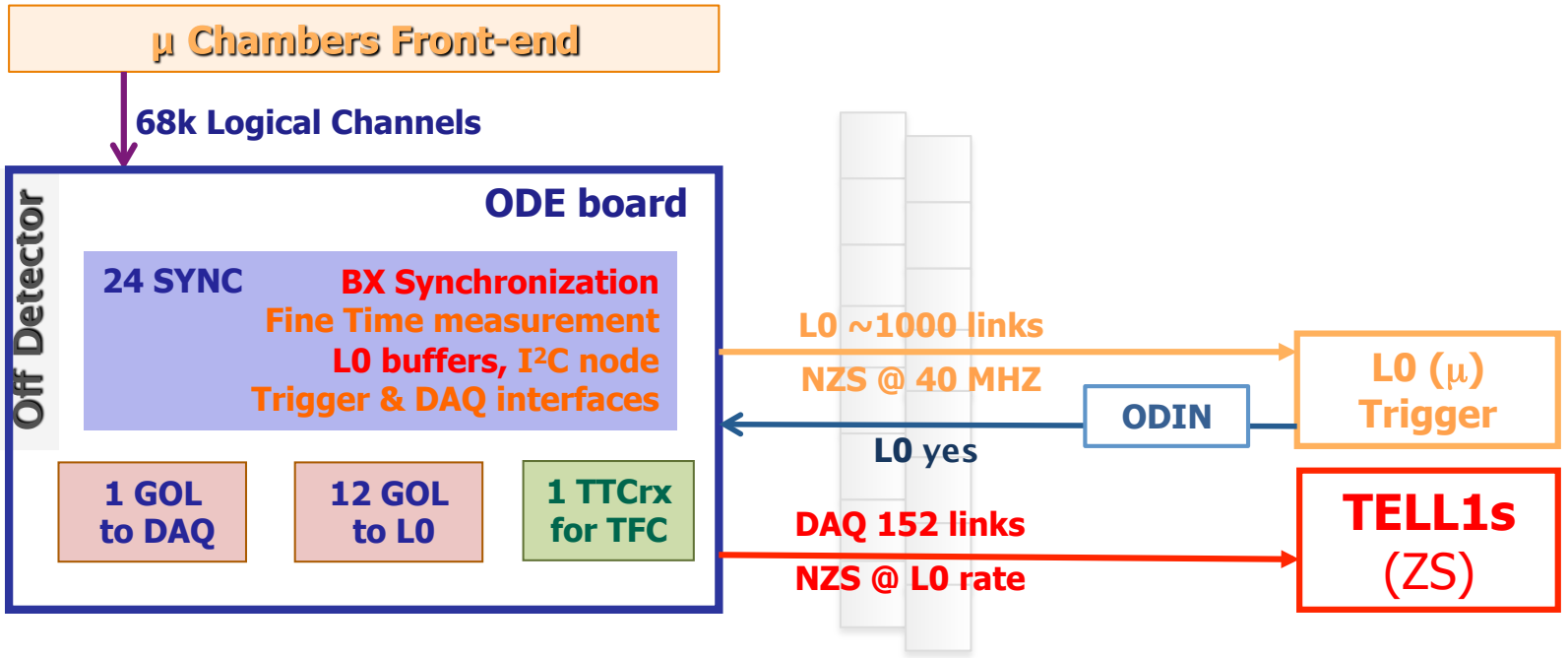


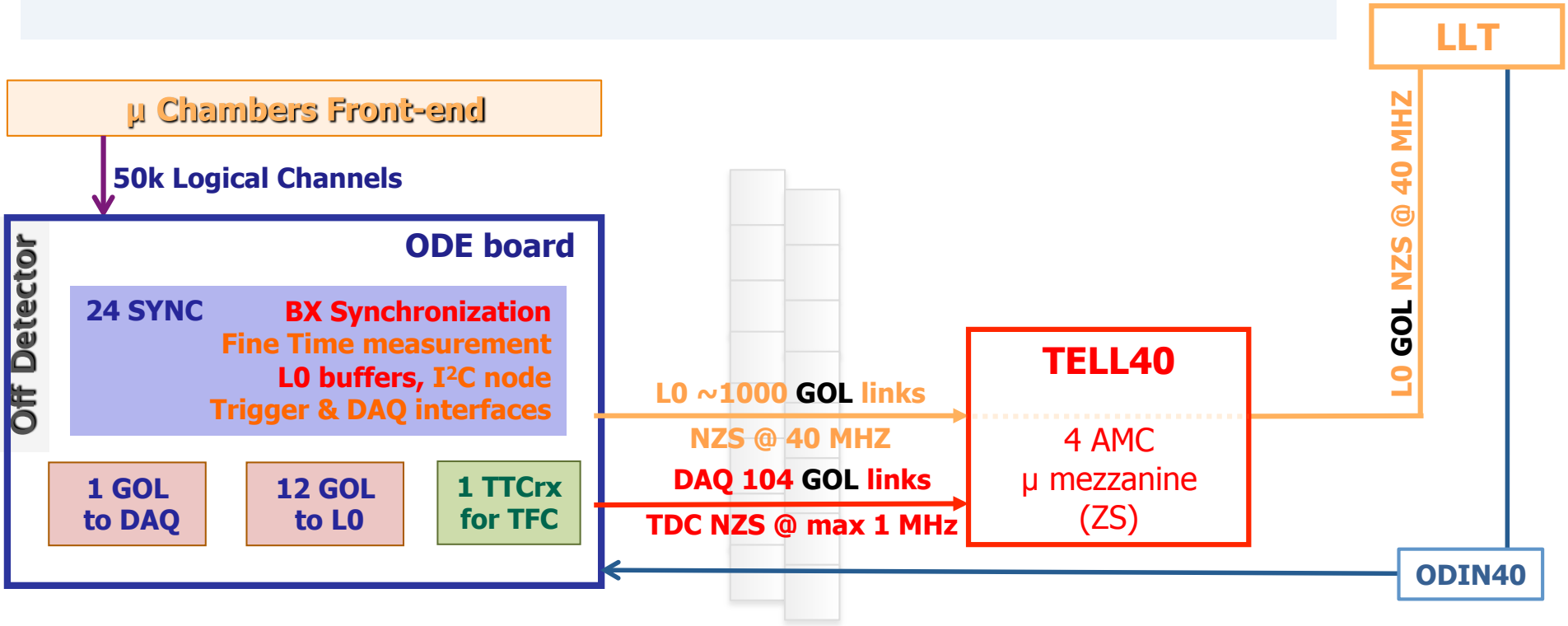
Present Architecture: Remarks

- The 4 bits **TDC information** is written on disk and is **very useful** to monitor and fine tune the time alignment of the Muon Stations
  - This information is sent from ODE boards to the Muon TELL1
    - @ max **1 MHz** with 1 GOL (~900 ns are needed to read back the ODE)
  - The events sent are selected by the **L0yes received** throughout the **TTCrx**
- **However** to reconstruct MUONS particles **only** the 1 bit **hit/channel** information is used
  - **Currently** this information is **extracted** from the **4bits TDC data** (max 1 MHz)
  - **But** the same type of information is sent **@ 40 MHz** from ODE boards to the L0 muon processors with the GOL

- **No ZS** is done **on ODE** boards
- The current implementation of the L0 muon trigger **does not consume** all the **L0 latency** (still ~ 20 step of 25 ns available)

Muon Electronics Upgrade

1. **4** μ stations: M2 M3 M4 M5
   → **104** ODE boards
2. **L0 link**: hit/channel information @ 40 MHz to **TELL40**
   → the information will be duplicated and send to the LLT
3. **DAQ link**: 4 bits TDC information to **TELL40** @ max 1 MHz
4. ECS communication via CANbus and ELMB



Starting points for the μ Upgrade

- L0 Muon trigger **will stay as in LHCb** (GOL/TTCrx data format)
- ODIN40 will emulate old TFC system
- M1 eliminated
  - From the **current 152 ODE** boards (M1 to M5)
  - To **only 104 ODE** boards (M2 to M5)
  - The M1 48 ODE could be counted as "spares"

- Under these hypothesis the muon electronics upgrade consists:
  - **No changes into the cavern**
  - **All modifications** to fit the upgrade requirements on the **TELL40 board**
    - Dedicated FPGA firmware (ACQ_MUON)

- Remarks **ODE side:**
  - TFC signals received on ODE with the TTCrx data format
  - Current L0yes became → Downscaled LLT @ max 1 MHz

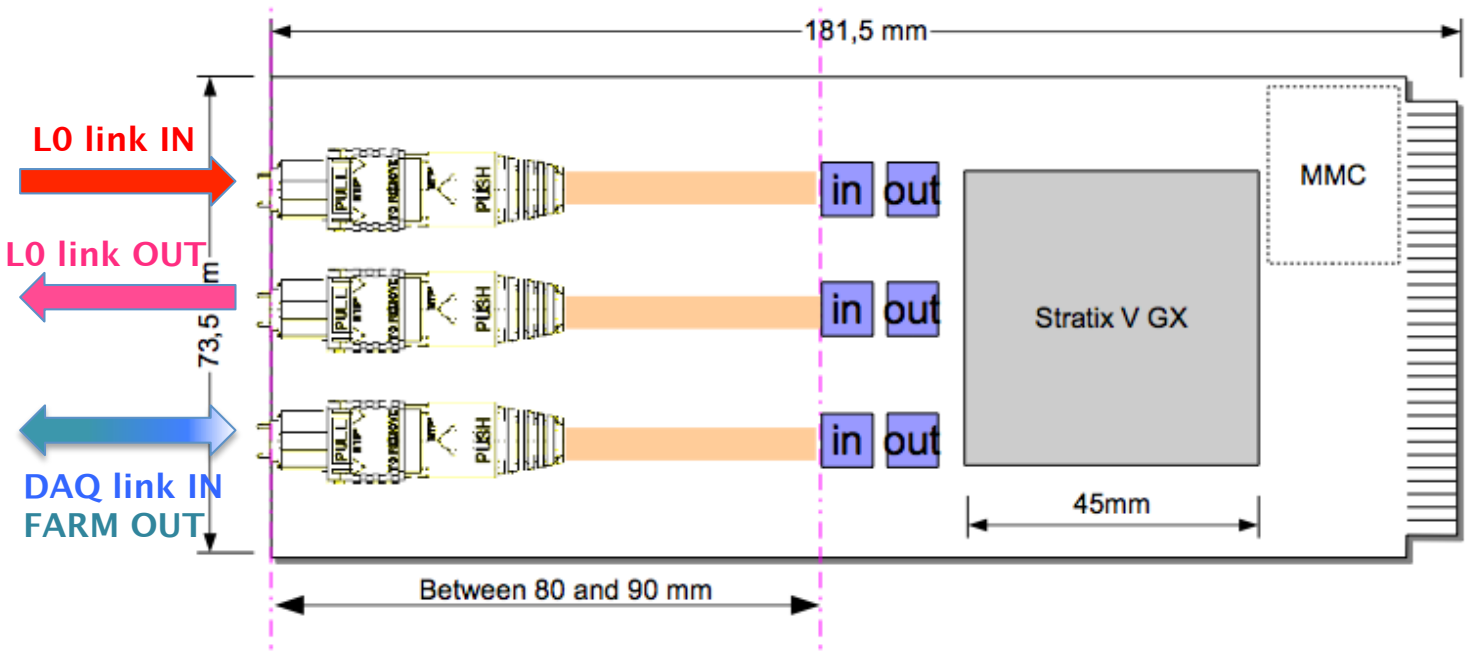
AMC Implementation

L0 links IN
12 links from ODE
32 bits @ 40MHz
GOL – 1.6 G bit/s

L0 links OUT
12 links to LLT
32 bits @ 40MHz
GOL – 1.6 G bit/s

DAQ link IN
1 link from ODE
36 words of 32 bits @ 1MHz
GOL – 1.6 G bit/s

FARM link OUT
1 links to FARM
10 G bit/s ethernet



- **AMC board**
  - 36 serial IN – 36 serial OUT
- **1 ODE corresponds to 1 AMC board**
  - The DAQlink bundles have to be divided in single fibers (In D3)

ODE/AMC/TELL40/crates

- ODE to TELL40 connection: **numbers**
  - 1 ODE board match 1 AMC board
  - 1 TELL40 crate → 10 TELL40 boars

  → **104 ODE** boards → **104 AMC** boards → **26 TELL40** boards

  → **4 TELL40 crates** if we want to take muon A and C sides independent

ACQ_Muon firmware

- Dedicated Muon firmware for the AMC FPGA
  - Duplication of the 12 L0link: inside the FPGA
    - We can use maximum 20 steps of 25ns to stay inside the LLT 4μs latency (not used by LLT)
    - De-serialize → copy → re-serialize the 12 links with the GOL data format
    - Fix the latency in the duplication of the link (input serial data to output serial data)
    - Only **the two LSB bits** of the Bunch Crossing Id are transmitted for each link
      - ✓ **Use the current L0 algorithm to verify the alignment of the L0linK?**
  - Zero Suppression
    - Provide a selectable ZS algorithm for each link type
  - Muon bank to be defined
    - Definition of information to be saved in the Muon banck (data/errors)
    - It is still necessary to extract the logical pad information as currently done for the HLT1?
    - Merge together the L0links and the TDClink in the same muon bank?

How many links to the farm?

- Muon TELL40 to the farm: 2 possibility to be investigated
- **Starting points**
  - L0data exit @ 40 MHz from the ODE board
  - **4 µs of LLT latency** to have the LLT trigger back to ODE board
  - ~ **1 µs** is needed to read back the TDCdata on the ODE board
  - On the ODE board up to 16 consecutive events can be stored
    → The corresponding TDCdata reach the AMC board in **16 µs**
  - Both L0data and TDCdata have the BXid information (at least partial)

1. **Simplest solution**
   - Exit to the farm with 2 independent links (L0data ; TDCdata)
2. **Merged solution (preliminary calculation)**
   - L0data must be stored on the FPGA to wait the TDCdata
     - for the maximum latency of **20 µs (is it too much??)**
     - **12 L0data links of 32 bit → 48 Byte @ 40 MHz**
     - A memory of minimum 20 µs / 25 ns = 800 row of 48 Byte → 38.4 k Byte

Conclusions

- All the electronics of the muon system will be reused in the LHCb upgrade with the current protocol scheme (GOL/TTCrx/1MHz trigger frequency)
- The only board which will be upgraded is the TELL1 → TELL40

- Two different data information will be recorded: an hit map @40 MHz (L0link) and the 4 bit TDC data @ 1 MHz (DAQlink)

- A dedicated muon firmware ACQ_Muon on the AMC FPGA is required to fit several requirements of the upgrade:
  - L0 link duplication for the LLT (GOL data format)
  - ZS algorithms
  - Muon banks definition (1 or 2 links per ODE: still do be decided)

- No PVSS hardware changes are foreseen → NO GBT link for PVSS data

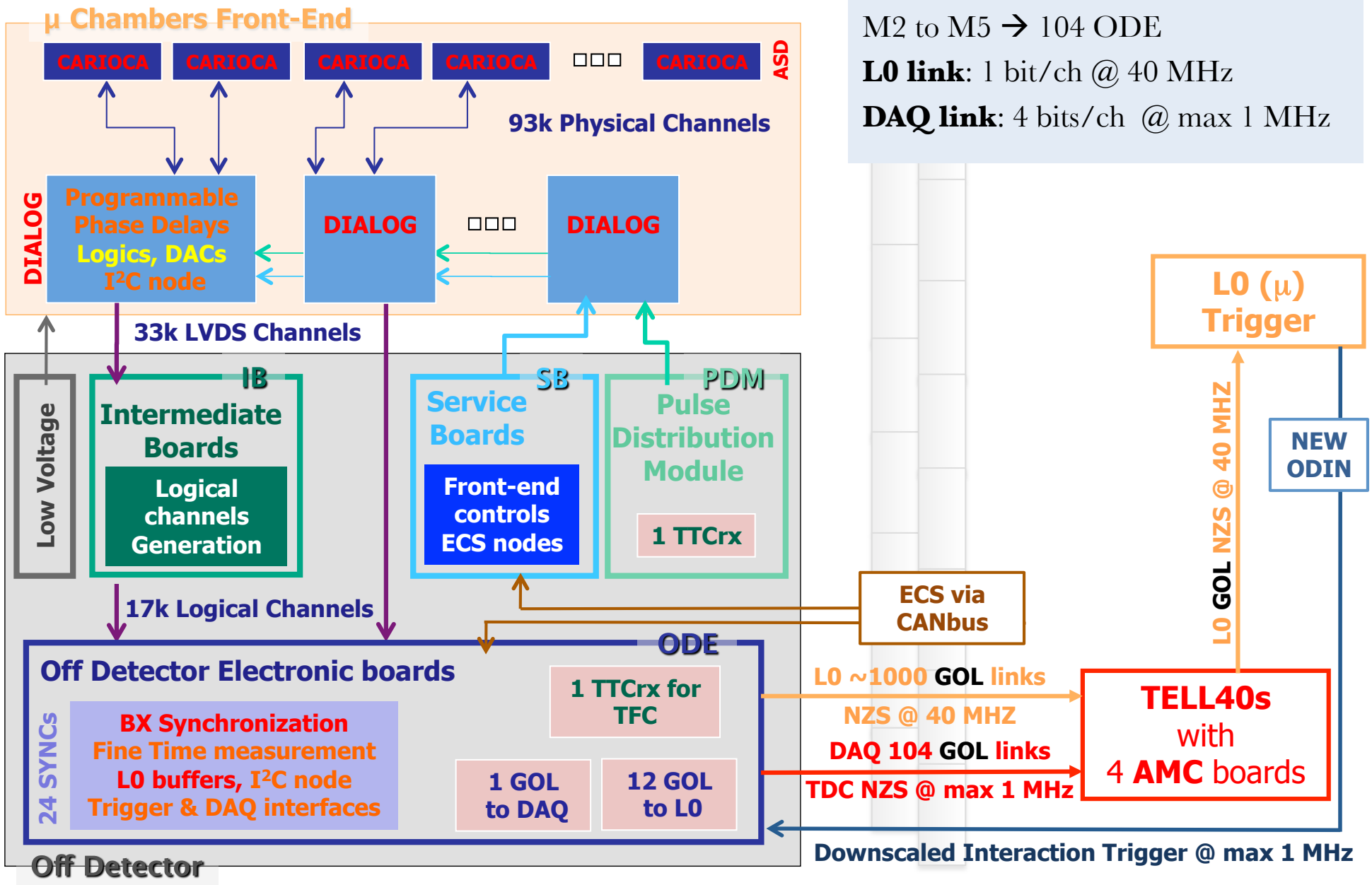
Conclusions

1. The estimated working-time to realize the ACQ_Muon firmware is ~ 1.5 man year once the specification will be available (end of 2011)
2. Currently it is still not clear if there is the man power to start this work before middle 2013, interest has been expressed from Frascati and Cagliari groups

3. Regarding the responsibility in terms of maintenance of the current muon electronics for all the LHCb upgrade (man-power, spares):
   - Elecronics
     - Cagliari INFN → DIALOG / SYNC / SYNC daughter board / CARDIAC board
     - CERN → CARIOCA TO BE CONFIRMED, BURKHARD? RIO (WHO?)?
     - Frascati lnf INFN → ODE board / Intermediated Board
     - Roma1 INFN → Service Board / PDM board
   - LV / HV
     - CERN → MARATHON WHO TAKE CARE? TO BE CONFIRMED?
     - → CAEN HV WHO TAKE CARE? TO BE CONFIRMED
     - PNPI → UF/PNPI WHO TAKE CARE? TO BE CONFIRMED

- MANPOWER A PARTE, NON MI E' CHIARO CHI METTA I SOLDI PER COMPRARE LE AMC BOARD, LE TELL40, I CRATE, LE FIBRE, IL COMMISSIONING

Muon Electronics Upgrade



M2 to M5 → 104 ODE

L0 link: 1 bit/ch @ 40 MHz

DAQ link: 4 bits/ch @ max 1 MHz

more in detail … ODE to TELL40

- **Output ODE → Input TELL40**
  1. **L0 links** @ 40 MHz from ODE (GOL data format); NZS 1 bit/channel information
     - 104 bundles of 12 fibers each
  2. **TDC link** @ 1 MHz from ODE (GOL data format); NZS 4 bits TDC/channel information
     - 104 single fibers (exiting from ODE) → grouped into 24 bundles of 12 fibers each

- Behavior of Muon TELL40 dedicated firmware **(AMC board)**
  - **Duplicate the L0link** (inside the FPGA)
    - The first link to be **forwarded to LLT** with the **GOL** data format
    - The second link is decoded and processed inside the FPGA
  - Than **FOR EACH link**:
    - **Z**ero **S**uppression if/where needed
    - Muon Bank definition to be studied

- **TELL40 Output →**
  1. **L0 links** @ 40 MHz **to LLT** (**GOL** data format)
  2. **DAQ link** to the farm