PACIFIC: SiPM Readout ASIC for LHCb Upgrade

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Introduction: LHCb

- Physics measurements limited by 1 MHz hardware trigger.
- Upgrade: increased luminosity, 40 MHz trigger at front-end.
- New detector for T1-T3: the Scintillating Fibre Tracker.

- 3 stations x 4 planes (x-u-v-x).
- 12 modules per plane.
- 6 layer fibre mats (mirrored).
- 8x2.5 m mats per module.
- 2 ROB (top/bottom) with 16 SiPMs and FE electronics.
Introduction: SciFi

- Ø250 µm scintillating fibres read by 128 ch SiPM array.
- Scintillation pulse time of arrival spreads over 15 ns.
- Low photostatistics yield inconsistent pulse shape.
- SiPM dead time exceeds clock period.
- Multichannel hit requiring clusterization (three threshold).

![Fibre Response Diagram](image-url)
Readout with 64 channel in CMOS 130 nm (IBM→TSMC).
Current mode input for direct anode connection.
Configurable non-linear digital output serialized.
Fast shaping to minimize spillover.
Signal integration to overcome low photostatistics using dual interleaved system to avoid dead time.
Single photoelectron detection capability.
PACIFIC: Preamplifier

- **Double feedback current conveyor:**
  - Fix input voltage and impedance.
  - Selectable gains at output mirror.

- **Transimpedance amplifier:**
  - Current to voltage conversion.
  - Control conveyor output voltage.

- Bandwidth 250 MHz.
- Input impedance 50 Ω.
- Input voltage control range 700 mV.
- Input dynamic range 4 µA-4 mA.
- Power consumption below 2 mW.
Double pole-zero cancellation scheme for fast shaping (10 ns).
Closed-loop OTA circuit with two configurable passive nets:
- First pole-zero net cancels slow component (SiPM capacitance and quenching resistor).
- Second pole-zero net cancels fast component (trace parasitics and input impedance).
A DC feedback loop controls the quiescent output voltage (critical for the subsequent integration).
PACIFIC: Integrator

- Classic closed-loop gated integrator architecture based on a Miller OTA with high slew rate.
- Dead times avoided by using two interleaved units with independent offset trimming circuits.
- Synchronization with the digitizer is mandatory.

Dual Gated Integrator
Dual passive track and hold merges the two subchannels.

Flash ADC using three PMOS comparators with:
- Dynamic range: 900 mV.
- Hysteresis: 10 mV.

Three independent references, configurable per channel, with:
- Dynamic range: 750 mV.
- Resolution: 8 bits.

The output of two channels is fed to a serializer that:
- encodes the three comparator outputs into 2 bits.
- streams out the output of two comparators with single-ended signal at 160 MHz.
PACIFIC: Additional features

- Internal bias current and voltage reference generation.
- Configuration memory bank with Hamming(7,4) coding.
  - Total of 339 registers, each 8 bit wide.
  - Self-corrected output (single flip).
- I²C slave for memory communications management.
- SEU notification, correction, counting and emulation.
- Analog debug outputs at Preamp, Shaper and T&H.
- Multi-channel internal/external charge injection system.
- Data pattern injection directly to serializer.
- Embedded 10 bit ADC providing ~3 kSa/s.
  - Wilkinson architecture operating on 3.33 MHz clock.
  - Dedicated external 1.2 V supply.
  - Intended for internal DAC characterization.
IBM Prototypes

- PACIFICr0 (May 2013):
  - Fix gain current conveyor.
  - Design migration from AMS 350 nm BiCMOS.

- PACIFICr1 (Nov 2013):
  - Analog FE + test blocks.
  - Analog external bias.
  - Independent GI output.

- PACIFICr2 (Aug 2014):
  - Eight full FE channels.
  - Internal biasing and I²C digital configuration.
TSMC Prototypes

PACIFICr3 (Jul 2015):
- First full size prototype.
- Separate bias left/right.
- DC correction mechanisms.

PACIFICr4 (Sep 2016):
- Wider integration window.
- Low comparator mismatch.
- Higher threshold resolution, configurable per channel.
Power and Bias

- Power consumption **9.4 mW/ch**, within specifications.
- Bandgap and derived reference voltages as expected.
- All voltage references use the same DAC design (6 bit) except the comparator thresholds (global & local) (8 bit).
- Reasonably linear response in all measured instances.
Input Voltage Control

- Derived from a resistor ladder with 16 possible values.
- Range (700 mV) and step (50 mV) as simulated.
- Four available gains are apparent.
- Good preamplifier linearity up to $\sim 40 \, \text{pC}$.
- Shaper peak voltage not as lineal, also limiting linear range to $\sim 30 \, \text{pC}$.

Measurement distorted by oscilloscope range change
Integration Window

- Over 15 ns of homogeneous integration.
- Observed spillover manageable by tracking software.
- Results from testbeam performed in Feb. 2107 at DESY.
SciFi light injection system pulse onto a fibre mat.
Distinct photoelectron structures are noticeable.
Processing channel architecture considered validated.
PACIFIC is a SiPM readout ASIC with:

- Current input for direct anode connection.
- Fast PZ cancellation shaping for tail suppression.
- Gated integrator damps statistical fluctuations.
- Non-linear configurable 2 bit digital output.

Channel architecture has been fully validated.

New prototype PACIFICr5 has been produced with:

- Differential output at 320 MHz, implying a reduction to 16 outputs with 4 channels per serializer.
- Input clock rate increased to 320 MHz.
- Extended comparator dynamic range down to 0 V, by changing devices to PMOS.
- Improved baseline restoration circuit at shaper output, compensating offset changes due to pulse rate variations.

Thanks a lot for your attention!