PACIFIC: LHCb Scintillator Fibre Tracker Readout ASIC

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***Abstract*—The LHCb detector will undergo a major upgrade during the Long Shutdown 2 (LS2), with the full replacement of the main tracking system. The new tracker will use scintillating fibres to cover the complete area of the detector. An array of silicon photomultipliers (SiPMs) will be used to readout these fibres. Each array will provide 128 channels, to be readout by the electronics. The low Power ASIC for the sCIntillating FIbres traCker (PACIFIC) is the readout ASIC designed specifically to cope with the readout of the Scintillating Fibre Tracker (SciFi). The 64 channel ASIC comprises for every channel analog processing, digitization, slow control and digital output at a rate of 40MHz. The analog processing includes preamplifier, shaper and integrator. The integrator is formed by an interleaved double gated integrator and a track and hold to avoid dead time (one integrator is in reset while the other collects the signal and the track and hold merges the two integrators output to give a continuous measurement). The output of the track and hold is digitized using 3 comparators (non-linear flash ADC). The three bits output is then encoded into two bits and serialized. Some auxiliary blocks are also needed to produce a fully functional device and include voltage references, current references, control DACs, power on reset (POR) circuitry and serializers. The slow control digital block consists in a 10 bit addressing I2C slave and a register bank for holding the configuration values. PACIFIC has been designed using TSMC 130nm technology and several prototypes have been validated. PACIFICr5 is expected to be the final prototype version with minor changes in the analog channel, some features added and a differential data link serializing the channels output at 320MHz.**

***Index Terms*—LHCb, ASIC, SEU, PACIFIC**

I. Introduction

The LHCb detector will be upgraded during the LS2 of the LHC in order to cope with higher instantaneous luminosity and to read out the data at 40MHz using a trigger-less read-out system. The current LHCb Tracking stations will be replaced by a single homogeneous detector based on scintillating fibres, covering the complete 5m×6m area of the detector[1]. The detector will be built from 2.5m long plastic fibres with a diameter of 250μm. The scintillation light is recorded with arrays of multi-channel SiPMs. Each SIPM sensor provides 128 channels, grouped in two silicon dies and packaged together. The electrical SiPM signals are then collected and processed by PACIFIC.

A. PACIFIC

PACIFIC is designed with a repetitive analog channel processing block connected to some analog bias block to set operating conditions and both of them controlled by a register file accessed via slow control (see figure 1). Each of the 64 channels in this ASIC comprises the analog processing, digitization and digital output at a rate of 40MHz (see figure 2). The analog processing includes preamplifier, shaper and integrator (see figure 2). The integrator is formed by an interleaved double gated integrator and a track and hold to avoid dead time (one integrator is in reset while the other collects the signal). The output of the integrator is digitized using three comparators (non-linear flash ADC). The three bits output is then encoded into two bits and serialized to be transmitted to a readout FPGA, used for clustering and data-compression. Data transmission between PACIFICr5 and FPGA is achieved by a fast serializer block that encodes 4 channels data (8 bits) using a 320MHz clock. Some auxiliary blocks are also needed to produce a fully functional device, including voltage references, current references, control DACs, power on reset (POR) circuitry and serializers. Additionally, the chip includes a digital block for slow control, composed of a register bank and an I^{2}C slave for communication.

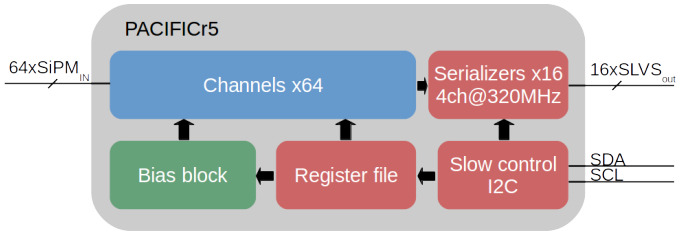

Fig. 1. PACIFICr5 blocks

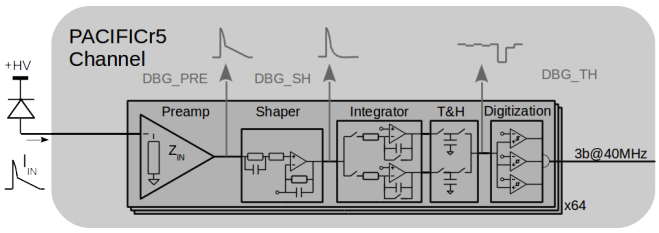

Fig. 2. PACIFICr5 analog processing chain

PACIFIC has been designed using deep sub-micron technologies and the actual implementation uses TSMC130nm

process. It will be available in a 256 pin BGA package needing only 12x12mm^2 area on the final carrier board.

PACIFICr3[2] was the first full size prototype providing real measurements of signals from 64 channels and including the analog processing, digital control and serialization. PACIFICr4[3] followed with some improvements and bug fixes to achieve better performance. This prototype was successfully tested in testbeam with the complete modules and a provisional DAQ. PACIFICr5 should be the final prototype version before production and was submitted in March 2017.

1) Slow Control: The output data from PACIFIC is processed by an FPGA and then transmitted using the GigaBit Transceiver (GBT) data link[4] provided by CERN. The GBT also provides a Slow Control Adapter chip[4] (GBT-SCA) for monitoring and slow control communication. The standard protocol chosen for the communication between the GBT-SCA and the ASIC is I^{2}C. The configuration will be stored in a set of registers that will be accessed through the I^{2}C slave implemented in the ASIC. This slave is based on a design provided by the Microelectronics section of the CERN PH-ESE group. It is fully compliant with the I^{2}C standard, using the 10 bit addressing mode introduced in Version 1 of the standard and multi-byte read and write commands based on the automatic increment of the address by the slave, both compliant with the GBT-SCA design.

B. Testbeam

In February 2017 a test-beam was performed at DESY using PACIFICr4b with 64 channels readout. As depicted in figure 3 the setup consisted in a reference telescope (provided by EPFL group) splitted in two parts. Each half of the reference telescope consists in two layers with x and y measurement. In the middle of the telescope two devices under test (DUT) are placed and readout by PACIFIC. The difference between the two devices is one is an irradiated module while the other is a non irradiated one.

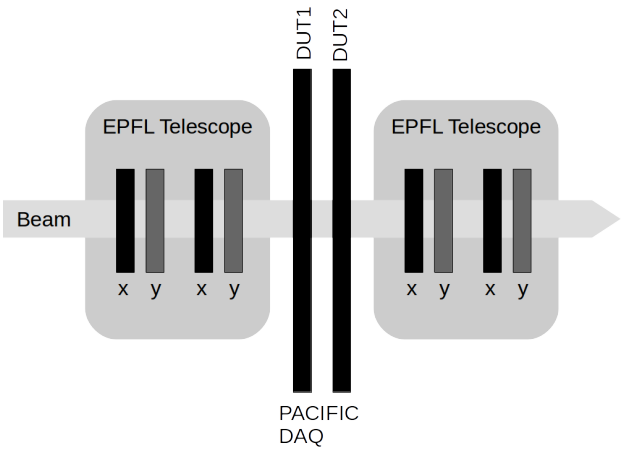

Fig. 3. Testbeam setup

The DAQ collects the data from both systems and time stamp it with a counter from the trigger generator (two scintillators in the particle path). Then the data is recorded with those timestamps indicating event identifiation to be able to merge the data afterwards. Since PACIFIC is not sensitive all the time to the signal (there is some unefficient integration close to the clock edges) the first thing is to select the events with correct integration. For this purpose a fine TDC on the DAQ FPGA is present. The date is fine time stamped so that inside a bunch crossing (25ns) the arrival time can be measured and the events selected.

1) Resolution: Using previous data and applying tracking algorithms the resolution can be estimated. For this purpose different beam energies where used during test-beam leading to a maximum resolution of 93.92μm at 6 GeV and degrading fast upto 272.88μm at 1GeV. The goal on the tracker is to achieve a resolution better than 100μm and does not seem a problem to obtain it.

C. Radiation environment

The environment on the detector is hard enough to take into account it's effects on the electronics. Taking into account expected accumulated dose [7] the main problem on the electronics may be the Single Event Upsets (SEUs) in the configuration registers. For this purpose a dedicated test at irradiation facilites at Heidelberg has been performed using standard methods [6] leading to a low enough cross section to avoid problems during opperation. The correction methods introduced in the prototype are enough to cope with the events flip expected during the lifetime of the detector.

II. Conclusion

A fully functional prototype tested in different conditions has been presented and is expected to be used on the detector. The overall functionality introduced in the prototypes is enough to cope with the different scenarios expected during the lifetime of the detector. The performance achieved on tests is good enough to validate the architecture and design of both the detector and the electronics together at the final detector.

References

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