PACIFIC: The Readout ASIC for the LHCb Scintillating Fibre Tracker

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***Abstract*—The LHCb detector will undergo a major upgrade during the Long Shutdown 2 (LS2) of the LHC, including the full replacement of the main tracking system.**

The new tracker will use scintillating fibres to cover the complete area of the detector. Arrays of silicon photomultipliers (SiPMs) will be used to readout these fibres. Each array has 128 channels and is read out by the low-power ASIC PACIFIC specifically developed for this purpose.

Each of the 64 channels of this ASIC comprise analog processing, digitization, slow control and digital output at a rate of 40 MHz.

The analog processing consists of a preamplifier, shaper and integrator. An interleaved double gated integrator avoids dead time as one integrator is in reset while the other collects the signal. The two integrator outputs are merged by a track and hold to provide a continuous measurement. The output voltage is digitized using 3 comparators acting like a non-linear flash ADC.

The three bits output is encoded into two bits and serialized (joining several channels). The design is complemented by auxiliary blocks such as voltage and current references, control DACs, power on reset (POR) circuitry and serializers. The slow control digital block consists in a 10 bit addressing I2C slave and a register bank for holding the configuration values.

The PACIFIC ASIC has been designed using a 130 nm technology and several prototypes have been validated. The recently tested PACIFICr5 is expected to be the final version. Compared to its predecessor the PACIFICr4b, only minor changes were applied to the analog channel, some features added and the channel output switched from a single-ended to a differential link which serializes the data at 320 MHz.

***Index Terms*—LHCb, ASIC, PACIFIC**

I. Introduction

The LHCb detector will be upgraded during the Long Shutdown 2 (LS2) period of the LHC in order to cope with higher instantaneous luminosity and to read out the data at 40 MHz using a triggerless read-out system. The current LHCb tracking stations will be replaced by a single homogeneous detector based on scintillating fibres, covering 12 detector layers of 5×6m ^{2} area[1]. It will be built from 2.5m long scintillating plastic fibres with a diameter of 250μm. The scintillation light is recorded by linear arrays of SiPMs. Each SiPM array has 128 channels with 0.25 mm pitch, grouped in two silicon dies and packaged together. The electrical SiPM signals are then collected and processed by the two PACIFIC ASICs with 64 channels each.

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A. The PACIFIC ASIC

The PACIFIC (low **P**ower **A**SIC for the s**CI**ntillating **FI**bres tra**C**ker) channel design is based on an analog processing block connected to an analog bias unit which allows to set the bias voltage of the SiPM. Both are controlled by a register file accessed via slow control. Each of the 64 channels in this ASIC includes analog processing, digitization and digital output at a rate of 40MHz (see figure 1). The analog processing features a preamplifier, a shaper and an integrator (see figure 1). The integrator is formed by an interleaved double gated integrator and a track and hold to avoid dead time (one integrator is in reset while the other collects the signal). The output of the integrator is digitized using three comparators, acting like a non-linear flash ADC. The three-bits output is then encoded into two bits and serialized to be transmitted to a readout FPGA, ensuring hit clustering and data compression.

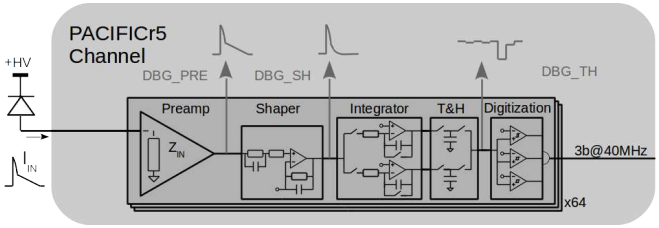

Fig. 1. PACIFICr5 analog processing chain (source: SciFi collaboration)

Data transmission between PACIFICr5 and FPGA is achieved by a fast serializer block that encodes 4 channels data (8 bits) using a 320 MHz clock. A set of auxiliary blocks complement the ASIC design such as voltage and current references, control DACs, power on reset (POR) circuitry and serializers. Additionally, the chip includes a digital block for slow control, composed of a register bank and an I^{2}C slave for communication (see figure 2).

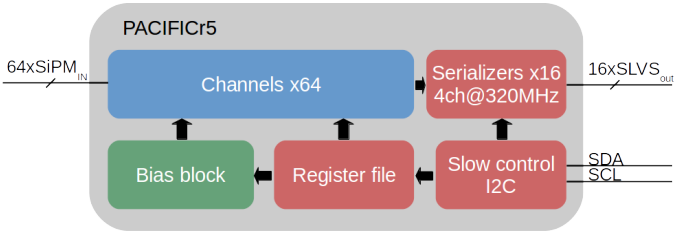

Fig. 2. PACIFICr5 blocks (source: SciFi collaboration)

The PACIFIC has been designed using deep sub-micron technology and the actual implementation uses a 130nm process. For its use in the SciFi tracker, it will be available in a 256 pin BGA package of only 12 x 12 mm^2 area on the final carrier board.

The PACIFICr3[2] was the first full size prototype providing real measurements of signals from 64 channels and including the analog processing, digital control and serialization. PACIFICr4[3] followed with some improvements and bug fixes for increased performance. This prototype was successfully tested in a particle beam with complete SciFi tracker modules and a provisional data acquisition (DAQ).

Readout and control: The output data of the PACIFIC is processed by an FPGA and then transmitted using the GigaBit Transceiver (GBT) data link[5] provided by CERN. The GBT also provides a Slow Control Adapter chip[5] (GBT-SCA) for monitoring and slow control communication. The standard protocol chosen for the communication between the GBT-SCA and the ASIC is I^{2}C. The configuration will be stored in a set of registers that will be accessed through the I^{2}C slave implemented in the ASIC. This slave is based on a design provided by the microelectronics section of the CERN PH-ESE group. It is fully compliant with the I^{2}C standard, using 10 bit addressing mode introduced in version 1 of the standard and multi-byte read and write commands based on the automatic increment of the address by the slave, both compliant with the GBT-SCA design.

II. Test results

The PACIFICr5 prototype overall performance has been characterized first with electrical tests and charge injection, and later with SiPM sensors, exposed to triggered light pulses. pulses[4].

The results are close to expectations obtained from detailed simulations and tests of previous prototypes. Figures 3, 4 and 5 show the analog signals at different stages from light pulses on the SiPM. The photon peak structure is clearly visible and allows to count the fired cells on the SiPM. The preamplifier reproduces the signal input shape, while the shaper reduces the tail. The Track and Hold output is the integrated result of the shaped signal during 25 ns.

A comparator threshold scan over its full range was performed at constant input light intensity. In figure 6 the average hit probability was plotted versus the threshold, which is usually referred to as 'S-curve'. The photopeak structure transforms into a step-like digital output. The light amplitude can be reconstructed by a differentiation of this curve, which is useful for absolute threshold calibration.

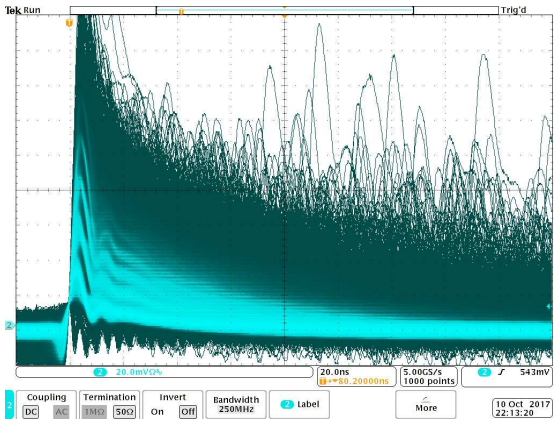

Fig. 3. PACIFICr5: Preamplifier output.

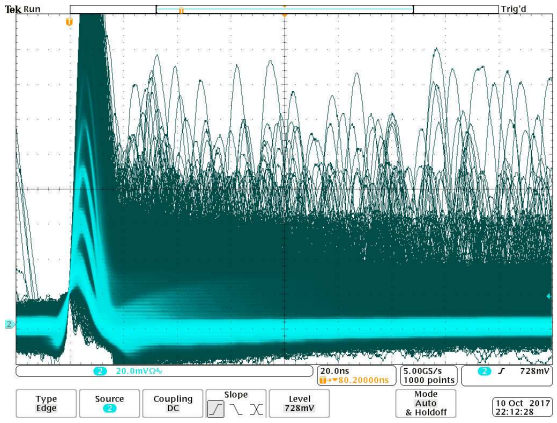

Fig. 4. PACIFICr5: Shaper output.

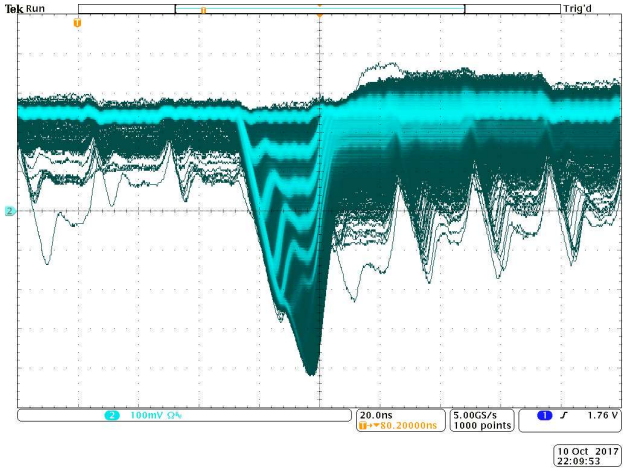

Fig. 5. PACIFICr5: Track & Hold output.

A. Testbeam

During 2017 two test-beam campaigns have been performed at the DESY test beam facility, using the PACIFICr4b and PACIFICr5 with 64 channels readout. The set-up consisted in a SciFi reference telescope split in two parts. Each half of the reference telescope featured two fibre layers for X and Y measurement. In the middle of the telescope two devices under test (DUT) were placed and read out by PACIFIC ASICs.

The DAQ collected the data from both systems and time stamped it with a counter based on two scintillation tiles which provided the trigger for the readout. The timestamps permitted event identification and later merging the data.

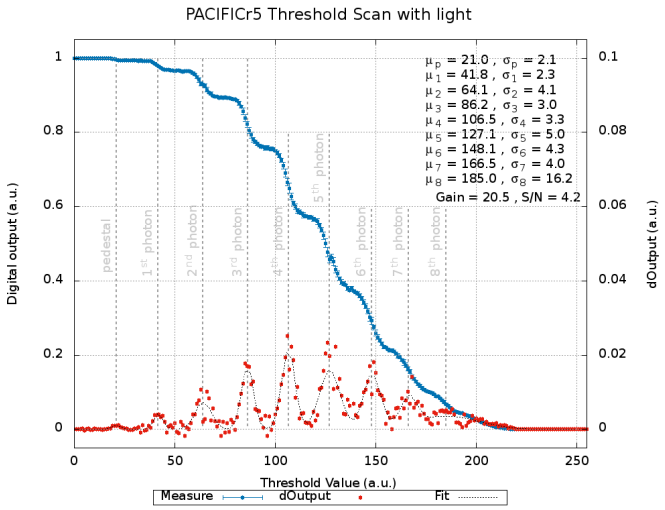

Fig. 6. PACIFICr5: Threshold scan with synchronous light injected (source: SciFi collaboration).

The integrators of the PACIFIC show some inefficiency close to the clock edges, leading to a time dependent sensitivity of the readout. Unlike at the LHC, the events at the DESY test beam arrive randomly in time. In order to select events which are correctly placed in the 25 ns time window (= hypothetical bunch crossing interval), a high resolution TDC on the DAQ FPGA was used. The data was fine-time stamped inside the 25ns window with 32 divisions.

Main results: With nominal SiPM gains and threshold configuration over the 64 channels in one PACIFIC, the overall detection efficiency was measured to be on average 99.3% .

Based on the same data, the hit resolution can be estimated from tracking algorithms. For this purpose different beam energies where used during test-beam. The hit residuals after clustering and track reconstruction have a sigma of 106 μm at the highest energy of 6 GeV, which is still limited by multiple scattering.

B. Radiation environment

The radiation environment in which the PACIFIC ASIC will operate is sufficiently harsh that radiation effects need to be considered. FLUKA simulations[7] predict an accumulated dose of about 50 Gy for an integrated luminosity of 50 $1/fb$. This indicates that Single Event Upsets (SEUs) in the configuration registers may be the main problem of the electronics. The correction methods (triple voting redundancy in slow control and Hamming encoding in configuration registers) introduced in the prototype have been tested and proven to be sufficient to cope with the events flip expected during the lifetime of the detector.

III. Conclusion

The PACIFICr5 ASIC is a fully functional prototype which was tested in different conditions and is expected to be used on the LHCb SciFi tracking detector. The overall functionality realised in the prototypes permits to cope with the different operational scenarios expected during the lifetime of the detector. The performance achieved in a range of tests validates the architecture and design of both the detector and the electronics.

IV. Acknowledgement

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). We would like to thank the DESY Test Beam Coordinators for their excellent help and the facility for the high beam uptime. Some test beam participants had travel funded by the H2020 project AIDA-2020 Transnational Access scheme, under GA no. 654168.

We would also like to thank the CERN PH-ESE group for their help and providing several pieces of source code and blocks for the PACIFIC design.

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