The Front-End electronics for the LHCb scintillating fibres detector
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LHCb downstream tracker upgrade

- The SciFi tracker is part of the LHCb upgrade to be installed in 2018 [1]
- Resolution < 100µm in bending plane
- Constrains on the electronics:
  - 40MHz readout (triggerless)
  - Tight geometry
- Radiation environment (≈ 80Gy at the location of the photo-detector)

Scintillating Fibre tracker layout

- 3 stations × 4 detection planes
- 12 modules per detection plane
- 16 SiPMs per module (width ≈ 530mm)
- Fibres read out at top and bottom

The fibres and the SiPM

- Fibres:
  - Scintillating fibres (≈250µm)
  - Mirror in the middle to improve the light yield
  - Module will have 5 or 6 layers of fibres

The Front End board

- PACIFIC: 128 channels ASIC with analog processing and digitization
- Clusterization FPGA to handle the digital processing (zero-suppression)
- Concentrator FPGA to optimize the bandwidth (1 for 4 SiPM)
- Modular design (maintenance and test)

PACIFIC: A 128 channels front-end ASIC

- Same granularity as the SiPM (128 channels)
- Prototypes designed in IBM 0.13µm
- Current conveyor with very low impedance input (≈ 25Ω)
- 4 Gains to handle various dynamic range: Dynamic range LSB (µA) Saturation
  - 0-15PE 12.5µA 0.8mA
  - 0-63PE 50µA 3.2mA
- (≈ 500mV) input voltage adjustment at 1.2V power supply
- Double pole-zero cancellation (SiPM decay: two times constants)
- Tunable shaper FWHM < 5ns (95 % of the charge < 10ns)
- Dual 25ns gated integrator (almost no dead time)
- 2 bits 40MS/s flash non-linear ADC
- 12µC, serializers based on CERN design
- Power consumption < 1W (8mW/channel)

Clustering algorithm

FPGA doing a simple barycenter computation with 4 thresholds:
- Seed threshold: Candidate for a cluster
- Neighbour threshold: With a seed, included in a cluster
- High threshold: Cluster, no others conditions
- Cluster sum threshold: Confirm a cluster

Conclusions

A baseline solution has been defined:
- PACIFIC for the analog processing and digitalization and FPGA for the digital processing
- Modular design for the FE board
- TDR submitted on 21/02/2014 to LHCC [2]
- Electronic review held on 10/12/2013

Perspectives:
- PACIFIC3 (change of technology), prototype of the FE board
- Integration studies (powering, clocks, optical links...)

References: