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Title: Prototypes and tests of the LHCb Scintillating Fiber detector front end electronics.

Summary
The Front-End (FE) electronics interfaces to the Silicon SiPMs on one side and to the experiment data-acquisition and control system on the other. All SiPM signals are amplified, shaped and digitized in the 64-channels PACIFIC ASIC; four PACIFIC ASICs are located on each PACIFIC Board. In order to reduce the data volume, the digitized channel data is routed to a flash-based IGLOO2 FPGA running a cluster-finding algorithm. Each Clusterization Board hosts two such FPGAs, processing the data of 256 PACIFIC channels. The cluster data is then further sent to GBTX serializers located on the Master boards; four Clusterization Boards are connected to one Master Board. A Readout Box (ROB) contains two Master Boards, eight Clusterization Boards, and eight PACIFIC Boards, and can service an entire SciFi module (2048 SiPM channels). The inter-connections between the three types of boards are realized through FMC connectors. The data serialized by the GBTX ASICs on the Master Board are shipped over optical fibers. The FE architecture is such that the cluster data of each SiPM are sent over a single fiber to the Back-End (BE) Electronics. Each ROB has also a complete interface for the distribution of bias voltages to the integrated circuits and to the SiPMs, of Timing and Fast Control (TFC) signals and of signals from and to the Experiment Control System (ECS). The communication with the TFC/ECS system goes via the GBT serial protocol: each Master Board hosts one Master GBT with an optical link connected to the LHCb SOL40 detector control system. The Master hosts also 11 FeastMP DC-DC converters, providing the necessary voltages to all devices in the ROB. Each ROB consumes about 100 W, and is individually cooled by demineralized water lines at 19C.

We produced and commissioned two ROB prototypes, including mechanical enclosure, cooling and shielding. We could successfully configure all devices on the ROB via the GBT serial links on the Master Board, using SOL40 firmware implemented on a prototype back-end electronics consisting of a mini-DAQ system based on the AMC40 architecture. In addition, we successfully demonstrated data transmission through the ROB, and could ship cluster data to the AMC40 mini-daq. We adopted the GBT "widebus" serial protocol at 4.48 Gbps, and a first implementation of the LHCb Tell40 DAQ framework in the AMC40, that processes incoming GBT data and produces 10GbE packets.

We were able to perform a complete system test and demonstrated that the design of the SciFi FE architecture is mature to pass to the production phase. A total of 288 ROBs are needed to service the entire SciFi detector (576 Master, 2304 Clusterization and PACIFIC Boards), for a total of about 590,000 readout channels. For the quality assurance of this large quantity of boards, a test system is under development. During production, this system, capable of injecting into each ROB channel a pulse with adjustable charge and time phase, will be able to provide a complete functional test.

Content
The on-detector electronics of the LHCb Scintillating Fiber Detector consists of multiple PCBs assembled in a unit called Read Out Box, capable of reading out 2048 channels with an output rate of 70 Gbps. There are three types of boards: PACIFIC, Clusterization and Master Board. The PACIFIC boards host PACIFIC ASICs, with pre-amplifier and comparator stages producing two bits of data per channel. A cluster-finding algorithm is then run in a FPGA on the Clusterization board. The Master Board distributes fast and slow control, and power. We describe the design,

production and test of prototype PCBs.