The Front-End electronics for the LHCb scintillating fibres detector

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The LHCb detector will be upgraded during the next LHC shutdown in 2018/19 [1]. The tracker system will have a major overhaul. Its components will be replaced with new technologies in order to cope with the increased hit occupancy and radiation environment. A detector made of scintillating fibres read out by silicon photomultipliers (SiPM) is studied for this upgrade. Even if this technology has proven to achieve high efficiency and spatial resolution, its integration within a LHC experiment bears new challenges. This detector will consist of 12 planes of 5 to 6 layers of $250\,\mu m$ fibres with an area of $5 \times 6\,m^2$. It leads to a total of 500k SiPM channels which need to be read out at 40 MHz. This article gives an overview of the R&D status of the readout board and the PACIFIC chip. The readout board is connected to the SiPM on one side and to the experiment data-acquisition, experimental control system and services on the other side. The PACIFIC chip is a 128-channels ASIC which can be connected to one 128-channels SiPM without the need of any external component. It includes the analog signal processing and a 2 bits non-linear flash ADC for digitisation. The PACIFIC chip design features a very fast shaping ($\approx 10ns$) and the ability to cope with different SiPM suppliers with a power consumption below 8 mW per channel.

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1. Introduction

The LHCb detector will be upgraded during the next LHC shutdown in 2018/19. It will have to run at an increased instantaneous luminosity of $5 \times 10^{32} \, cm^{-2} s^{-1}$. As concerns the tracker system, it will have a major overhaul in order to cope with the increased hit occupancy and radiation environment. In this regard, a detector made of scintillating fibres read out by silicon photomultipliers (SiPM) is studied for the downstream tracker upgrade (called SciFi tracker). Its position within the LHCb detector is shown on the left of Fig.1. It will consist of three stations (T1-T3) of 4 planes, each with 5 to 6 layers of $250 \, \mu m$ scintillating fibres. Its area is $5 \times 6 m^2$. The expected hit resolution is less than $100 \, \mu m$ in bending plane.
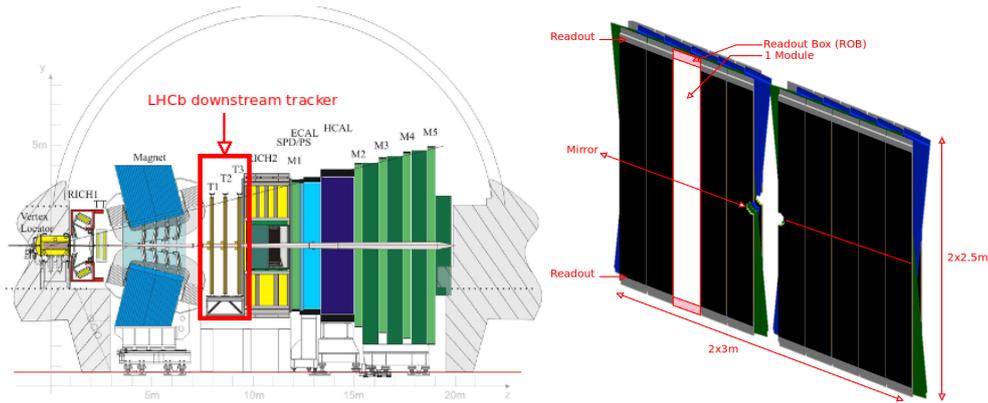

Figure 1: The current LHCb detector and the location of the downstream tracker (left) and details of the first station (right)

The Fig.1 (right) shows the details of one station with the half-planes moved apart. Each plane is split in 10 to 12 independent modules of $\approx 530mm$. The readout box (ROB) containing 16 SiPM and the front end electronics is located at the top and the bottom part of the detector. A mirror is placed at the end of the fibres (in the middle of the detector) in order to improve the light yield.

In total, about $140 \, m$ are instrumented with scintillating fibres which leads to 560k channels of $250 \mu m$ width (4352 SiPM).

2. The SiPM

The SciFi tracker uses 128 channels SiPM. They are well suited for this application as they exhibit a fast signal response combined with a fast recovery. The simulation for 1 minimum ionizing particle hit near the mirror (middle of the detector) after irradiation gives a light yield of 13.7 PE for 5 layers of fibres and 16.6 PE for 6 layers of fibres.

Several SiPM providers are investigated. The signals from the SiPMs by KETEK [1] and Hamamatsu [2] is given on Fig.2. As it can be observed, they exhibit very different signal shapes depending on their design and technology. For the examples given, the Hamamatsu SiPM recovers in $\sim 50ns$

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[1] KETEK GmbH, Hofer Str. 3, 81737 Mãijnchen, Germany.

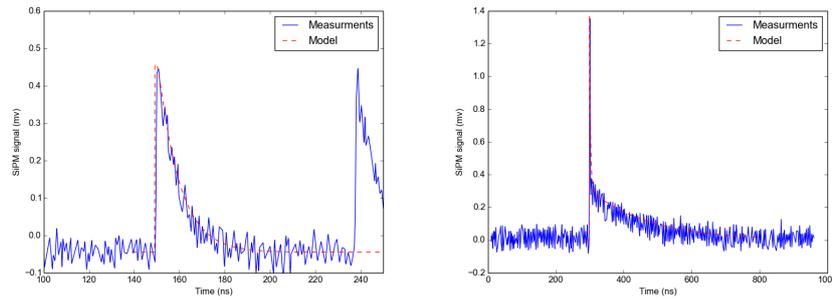[2] Hamamatsu Photonics K.K., 325-6, Sunayama-cho, Naka-ku, Hamamatsu City, Shizuoka Pref., 430-8587, Japan

Figure 2: Sample signal from an Hamamatsu SiPM (left) and Ketek SiPM (right), the acquired signal on 50Ω is in blue and its model in red

while the Ketek SiPM signal has a very fast and sharp answer but recovers in $\sim 250\,ns$. Moreover, their amplitudes are quite different ($1.4\,mV$ against $0.5\,mV$).

Therefore, the front end chip will have to be versatile and able to cut the long tails before the digital processing.

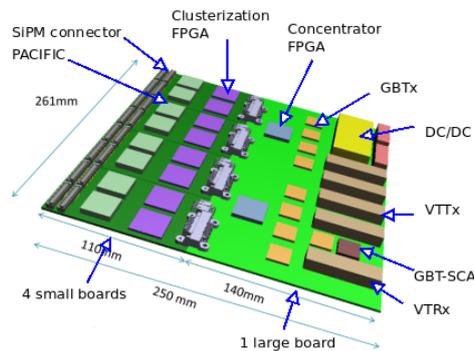## 3. The Front End board

Figure 3: Possible FE board

The front end board is connected to the SiPM on one side and to the service, the slow control and the data acquisition (DAQ) on the other side. A possible design for the FE board is given on Fig.3. The design is modular in order to ease the maintenance and the tests.

The SiPM are connected with a flex cable to the FE connector. Their output signal is processed using a dedicated front-end chip (PACIFIC), then a FPGA handles the zero suppression. It consists in computing the barycenter of the signal deposit and sends the results to concentrator FPGA which allows to optimize the bandwidth depending on the detector occupancy. Finally, the data is sent using the GBTx chip and optical links to the DAQ [3]. A GBTx/GBT-SCA allows to receive and distribute the slow control and the clocks to the FE chips.

The board is powered using the DC/DC converters developed at CERN [4].
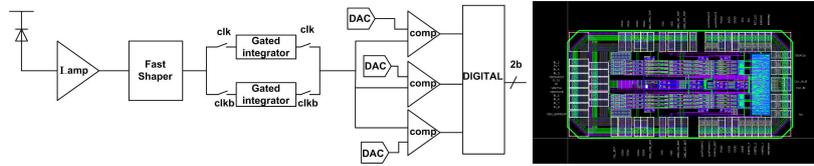
4. PACIFIC: A 128 channels front-end ASIC

Figure 4: Synoptic of the PACIFIC analog processing and its realization in the the IBM $130\,\mu m$ technology

The PACIFIC chip is developped in order to have the same granularity as the SiPM (128 channels). The first two prototypes (one and eight channels) have been developed in IBM $130\,nm$. Its synoptic is given on Fig. 4.

Its first stage is a current conveyor with a very low input impedance ($\approx 25\,\Omega$). It can be configured with 4 gains to handle various dynamic ranges (saturation between $0.8\,mA$ and $3.2\,mA$).

The input stage can also adjust the SiPM bias voltage within $0-500\,mV$ at $1.2\,V$ power supply. It is followed by a tunable shaper, with a fully configurable double pole-zero cancellation. It allows to cancel the SiPM exponential decrease in order to have a $FWHM < 5ns$ (95 % of the charge $< 10ns$). The dual $25\,ns$ gated integrator processes the signal before its digitization by a 2 bits 40MS/s flash non-linear ADC.

The target power consumption for 128 channels is $< 1W$ ($8mW/channel$).

5. Conclusions

A baseline solution has been defined with PACIFIC for the analog processing and digitalization and two stage of FPGA for the digital processing. The FE board design has been kept modular. This solution has been reviewed on 10/12/2013 and included in the TDR submitted on 21/02/2014 to the LHCC [2].

The work will now be emphazed on the third version of the front end chip (PACIFIC3) with a change of technology and on the development of the first prototypes of the FE board. In the meanwhile the integration issues are studied (powering, clocks, optical links...).

Acknowledgments

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References

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[3] P Moreira et al., *The GBT project* (https://cds.cern.ch/record/1235836?ln=fr)

[4] F.Faccio et al., *Development of custom radiation-tolerant DCDC converter ASICs*, Journal of Instrumentation, Vol.5, December 2010