PACIFIC: SiPM Readout ASIC for the LHCb Upgrade
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The LHCb Upgrade

- Factor 5 higher luminosity.
- Triggerless 40 MHz readout.

New tracking system:
- Vertex detector: Si strips → pixels.
- Upstream tracker: Si strips → Si strips (larger coverage).
- T1-T3 tracking station: Si and straws → Scintillating Fibre Tracker (SciFi).
Overview of the SciFi

- Scintillating Fibre Tracker:
  - 3 stations × 4 planes (x-u-v-x).
  - 128 modules (0.5 × 5 m²).
  - 11,000 km of fibres, 524 kChannels.
  - Readout electronics at the top and the bottom of each module.

- Performance:
  - Light detector, < 1% $X_0$/layer.
  - Hit efficiency $\approx$ 99 %.
  - High granularity 250 µm, hit resolution < 100 µm.
  - Total radiation up to 35 kGy near the beam pipe, 60 Gy for the electronics.
Overview of the SciFi

- Each module is composed of 8 fibre mats:
  - Length: 2.4 m.
  - Stack of 6 fibre layers.
- Double-cladded scintillating fibres (Kurukay, SCSF-78, $\varnothing$ 250 µm)
- Each mat is readout by 4 silicon photomultiplier:
  - 128 channels/SiPM.
  - 250 µm channels.
Working principle

- A ionising particle traversing the scintillating fibres produces scintillation light spreading over 15 ns.
- SiPMs collect the light and generate a signal.
- Low photo-statistics yield inconsistent pulse shape.
- SiPM dead time exceeds clock period.
- The particle position is calculated by a weighted mean of the signal in the cluster.
FE electronics

Readout electronics:

- SiPM sensor on Flex cable.
- PACIFIC carrier board.
  - Analog processing.
  - Digitization.
- Cluster board.
  - Clusterization algorithm.
  - Fast control handling.
  - Pack the data.
- Master board.
  - Power supplies.
  - Optical links.
Available bandwidth:

- PACIFIC digitization
  \[2 \times 2b \times 64@40MHz\]
- Zero suppression (ZS) algorithm:
  \[20.48\text{Gb/s} \rightarrow 4.48\text{Gb/s}\]
- GBT: 112b@40MHz
  \[4.48\text{Gb/s}\]
- TELL40: 24 or 48 GBT inputs
- 16 \times PCIe v3.0 output allowing 110Gb/s

**Figure:** Bandwidth available at each processing stage
Clusterization algorithm

The clusterization algorithm:

- Processing done in the clusterization board FPGA (Microsemi IGLOO2).
- 128 inputs $\times 2b$ (SiPM size, the gap between SiPM forbid overlapping algorithm).

Use 3 thresholds:

- **Seed threshold**: Candidate for a cluster
- **Neighbour threshold**: With a seed, included in a cluster
- **High threshold**: Cluster, no others conditions

A cluster is confirmed the sum of the seed and neighbouring channel is over the *cluster sum threshold*. 

**Figure**: Example of clusters
Channel processing chain:

- Current input.
- Anode voltage control.
- Fast Shaper for tail adjustment.
- Double interleaved gated integrator.
- Track and hold.
- Digitization with 3 hysteresis comparators.
- Serialization at 320 MHz.
PACIFIC: Preamplifier

- Double feedback current conveyor:
  - Fix input voltage and impedance.
  - Selectable gains at output mirror.
- Trans-impedance amplifier:
  - Current to voltage conversion.
  - Control conveyor output voltage.

- Bandwidth: 145-255 MHz depending on the gain.
- Input impedance: 50 Ω.
- Input voltage control range 500 mV.
- Input dynamic range: 4 µA-4 mA.
- Power consumption below 2 mW.

![Diagram of a preamplifier with labels for various components such as V_{offset}, I_b, I_{bfk}, and V_{out}. The diagram includes feedback loops for LF and HF, and an external node connected to the output.]
The SiPM signal exhibits two exponential decay:
  - Double pole-zero cancellation scheme for fast shaping (FWHM: 4.5-5.8 ns).
  - Closed-loop OTA circuit with two configurable passive nets:
    - First pole-zero net cancels slow component (SiPM capacitance and quenching resistor).
    - Second pole-zero net cancels fast component (trace parasitics and input impedance).
  - A baseline holder is used to reduce the random fluctuations of the SiPM signal.

![Double PZ Shaper](image-url)
PACIFIC: Digitizer

- 3 comparators with a mean hysteresis of 10 mV.
- Thresholds adjustable individually with an 8 bit resolution.
- Allows to keep the discrepancy between channels bellow 1/4th of a PE.
PACIFIC: Additional features

Slow control:

- I\(^2\)C slave for memory communications management (protected using TMR).
- 338 registers (8 bits) are used to configure the chip.
  - Use Hamming(7,4) coding.
  - Self-corrected output (single flip).
- Single-Event Upset (SEU) notification, correction, counting and emulation.

Testing features:

- Debugging outputs at Preamp, Shaper and T&H allowing to spy each channel.
- Multi-channel internal/external charge injection system.
- Data pattern injection directly to the 320 MHz serializer.
- Embedded 10 bit Wilkinson ADC providing \(\sim 3\) kSa/s.
  - Intended for internal DAC characterization.
Results: Typical SiPM signal

- SiPM signal observed with the Pacific debugging outputs.
- All channels triggered using a synchronous light.
- Can follow the signal path.
- Works as expected.
Results: S-Curves

- After the digitization.
- All channels triggered using a synchronous light.
- DAC threshold moved from 0 to 255 (threshold scan).
- PE peaks visible and separated.

Some light:

More light:
Two test beam campaigns at DESY (February and August 2017).

Two SciFi modules installed.

Equipped either with a Pacific or a Spiroc readout.
Results: Test beam 2/3

- Using a 6 GeV energy run.
- Single hit residuals after the cluster barycentre processing:
  - Spiroc readout: 114 µm.
  - Pacific readout: 112 µm.
Results: Test beam 2/3

Efficiency computed after the cluster barycentre processing:

- Comparable between Spiroc and Pacific
- Using irradiated and un-irradiated SiPM

Spill-over issue spotted:

- Due to the track and hold
- Bottom-plate sampling implemented in the production version of Pacific.
The LHCb SciFi is a high resolution tracker covering 340 m$^2$ based on 250 µm diameter scintillating fibres.

A solution for the FE electronics has been developed:

- 2 PACIFIC per SiPM package with the analog processing and digitalization.
- Dedicated FPGA for the clusterization.
- Modular design for the FE board

PACIFIC is a SiPM readout ASIC with:

- Current input for direct anode connection.
- Fast PZ cancellation shaping for tail suppression.
- Gated integrator damps statistical fluctuations.
- Non-linear configurable 2 bit digital output.

PACIFIC architecture has been fully validated.

Production has started, first batch of FE boards for July
Thanks a lot for your attention.
PACIFIC Prototypes

- PACIFICr0 (May 2013):
  - Fix gain current conveyor.
  - Design migration from 350 nm BiCMOS.

- PACIFICr1 (Nov 2013):
  - Analog FE + test blocks.
  - Analog external bias.
  - Independent GI output.

- PACIFICr2 (Aug 2014):
  - Eight full FE channels.
  - Internal biasing and $I^2$C digital configuration.
PACIFIC Prototypes

**PACIFICr3 (Jul 2015):**
- First full size prototype.
- Separate bias left/right.
- DC correction mechanisms.

**PACIFICr4 (Sep 2016):**
- Wider integration window.
- Low comparator mismatch.
- Higher threshold resolution, configurable per channel.