Summary of Decisions Taken at the Baselining Workshop

Introduction

To define the baseline for two critical topics for the detector readout and powering, two taskforces have been run between October 2018 and February 2019. The options for reading out the data from the front-end chips have been evaluated in the "High-Speed Data Transmission Taskforce" and the powering system of the serial powering chains has been investigated in the "Serial Powering Taskforce". Reports from the taskforces including their recommendations have been presented and discussed at a Baseline Workshop, taking place on 4.-5. March 2019 at CERN: https://indico.cern.ch/event/801168/

This document summarizes the baseline decision taken by the ITk pixel coordination group and the reasoning.

Data transmission baseline

The data transmission between the modules and the off-detector FELIX cards is performed electrically in the innermost part and optically in the other part. As the old baseline using an aggregator ASIC at PP0 is obsolete due to several reasons (cooling of PP0 in the inner system, no design effort started for the ASIC, …), new transmission path implementations have to be investigated.

Two transmission options have been identified to be viable for reading out the detector, the *direct transmission* and *fibre inside* option. Both options have been studied in detail during the taskforce work and advantages and disadvantages, risks and benefits have been addressed. With the currently obtained knowledge, both options seem to be working. But both options need a lot of additional work to be studied in detail and proven to be working with a real system. As this is not possible to be done within the time of taskforce, estimates on the likelihood and the risk have been taken as a measure for making a baseline decision. The interpretation of risks turned out to be a critical point, especially because of a non-existing baseline schedule against which a schedule risk can be estimated. The taskforce therefore did this for both options in the same way, but it has to be stated, that once a schedule is defined and further studies are done, the risk matrix has to be revisited. Nevertheless, as there is not enough manpower and time to follow both transmission options in full detail, the taskforce had to recommend one of the options.

The final recommendation, which is supported by a majority of the taskforce, is the *direct transmission* option, which has been identified to provide the lower risk for the project.

The discussion during the baseline workshop followed this recommendation as to be the one which can be implemented for the full detector system without immediately obvious show-stoppers. It aims for a mainly passive and not cooled PP0 area and a simpler engineering of the inner part of the detector at the cost of having more cables and with this more material in the pixel detector volume.

The detailed baseline decision is to implement the data transmission as direct electrical links in between the front-end ASICs and the optoboards which are to be located at the ITk endplate *and* in between the LAr feedthrough boxes. The cables in between are baselined to be MOLEX TwinAx AWG34[1] cables which come with a polyethylene (LDPE) dielectric which needs to be confirmed with TC to be allowed to be installed as it is flammable. A derogation request has been started on this already before the Taskforce work.

To save cables and with this material, the link sharing of data inside a module might be used. RD53B will offer a 320 Mbps link sharing in between FE-chips. In the L1 flat region this link sharing is set as baseline and in the L4 flat region as mitigation option. Further studies of bandwidth are needed to check if more detector parts can profit from this. ITK pixel will push the RD53B specifications towards providing a 640 Mbps link sharing. In any case, baseline is to install all the needed links and fibres for the 4 MHz readout case without relying on a heavier use of link sharing for the 1 MHz readout case.

No link sharing for the downlink is baselined, because of missing evidence of a good performance in terms of jitter for the future ASICs. Nevertheless, to provide a mitigation option for reducing services if needed, the downlink-sharing should be implemented on the Type-0 services by including the necessary connections into the design.

The optoboards will be powered by an on-board DC-DC-converter and incorporate an active equalizer ASIC to receive the detector data. As this will need more space for the boards, space in between the LAr feedthrough boxes will be used for optobox placement.

Powering baseline:

The serial powering taskforce has discussed in detail the necessity of including the PSPP chip with the bypass in the detector; after an assessment of the associated risks, the taskforce has recommended not to include the bypass in the PSPP chip. The justification for removing this safety feature from the detector is heavily based on new design features of the Shunt-LDO regulators in the production version of the front-end chip: An undershunt-current protection mechanism will reduce the chip core voltage if necessary in order to prevent overloading the regulator and causing transients on the LV line, and an on-chip voltage if clamp will be connected in parallel to the regulator to protect the chip from overvoltage. The ITk Pixel Community has expressed its confidence that the design specifications for these critical elements of the Shunt-LDO regulator will be met and has therefore chosen to follow the recommendation of the serial powering taskforce.

At the same time, while during shutdowns the environmental temperature sensors in the gas volume in combination with the interlock sensors are sufficient for monitoring the temperature of the sensors for annealing studies, the community has deemed the monitoring capabilities of the PSPP chip (module temperature and module voltage monitoring) important not only for a safe operation of the detector over the planned long term, but in particular during the integration and commissioning phase. The importance of a separate, independent data path for this monitoring path has also been pointed out by the serial powering taskforce. The implementation of this control path by means of the PSPP chip has however been identified as too complicated – it has been decided that without the bypass, the current powering scheme

[1] TwinAx cable data-sheet of the commercial item:
https://www.molex.com/molex/search/partSearch?query=100068&pQuery=

of the PSPP is too power hungry and too complicated to justify including the PSPP chip just for monitoring. It was decided not to include a PSPP chip per module in the baseline.

The ITk Pixel Community has therefore decided to change the design of the DCS controller chip, which is located at PP0, in order to employ this chip for monitoring the module temperature and module voltage. A single DCS controller per serial powering chain, with two wires for powering and two wires for communication to the off-detector DCS, located at PP0, has hence been included in the baseline.

For the diagnostics path, the FE-ASIC needs to read one of the module's NTCs for temperature monitoring through the data transmission path.

Summary

In summary, the baseline decisions for the services implementation need to be studied in detail and the design of components has to be performed. Each of the sub-systems must show the feasibility of fitting all the services into the available envelope. The optoboard and optobox designs are to be done including its powering scheme and the serial powering system is to be tested with the final RD53 Shunt-LDO without the PSPP safety mechanism, first as test chip and finally with the complete ASIC.

The risk register is to be updated based on the decisions taken, the identified risks and their mitigations.

The services specification including the baseline is to be updated and reviewed in the SPR. Finally, the schedule will be reworked to include the baseline for the services implementation.

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