# CERN GTK Demonstrator ASIC Update

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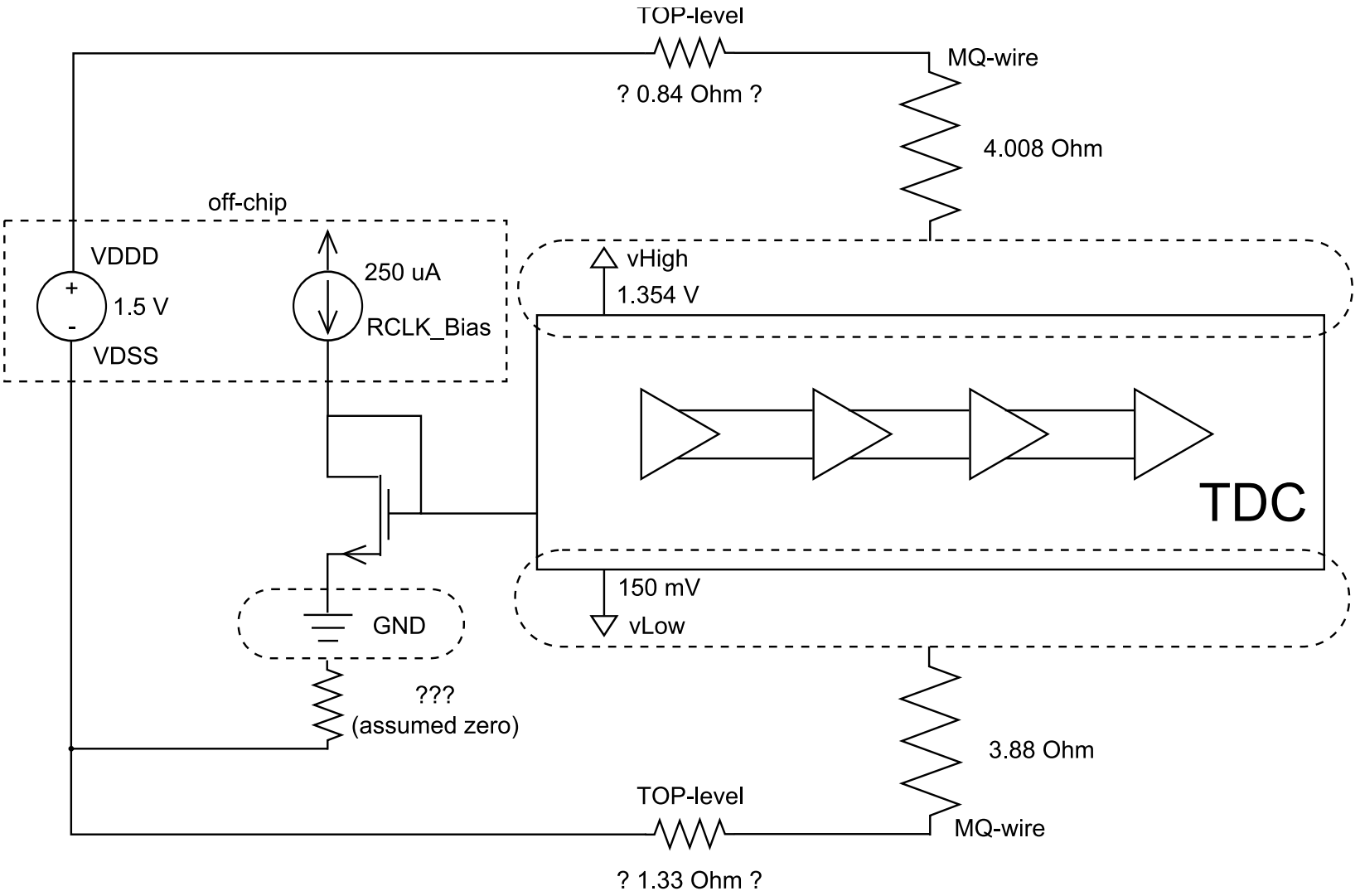
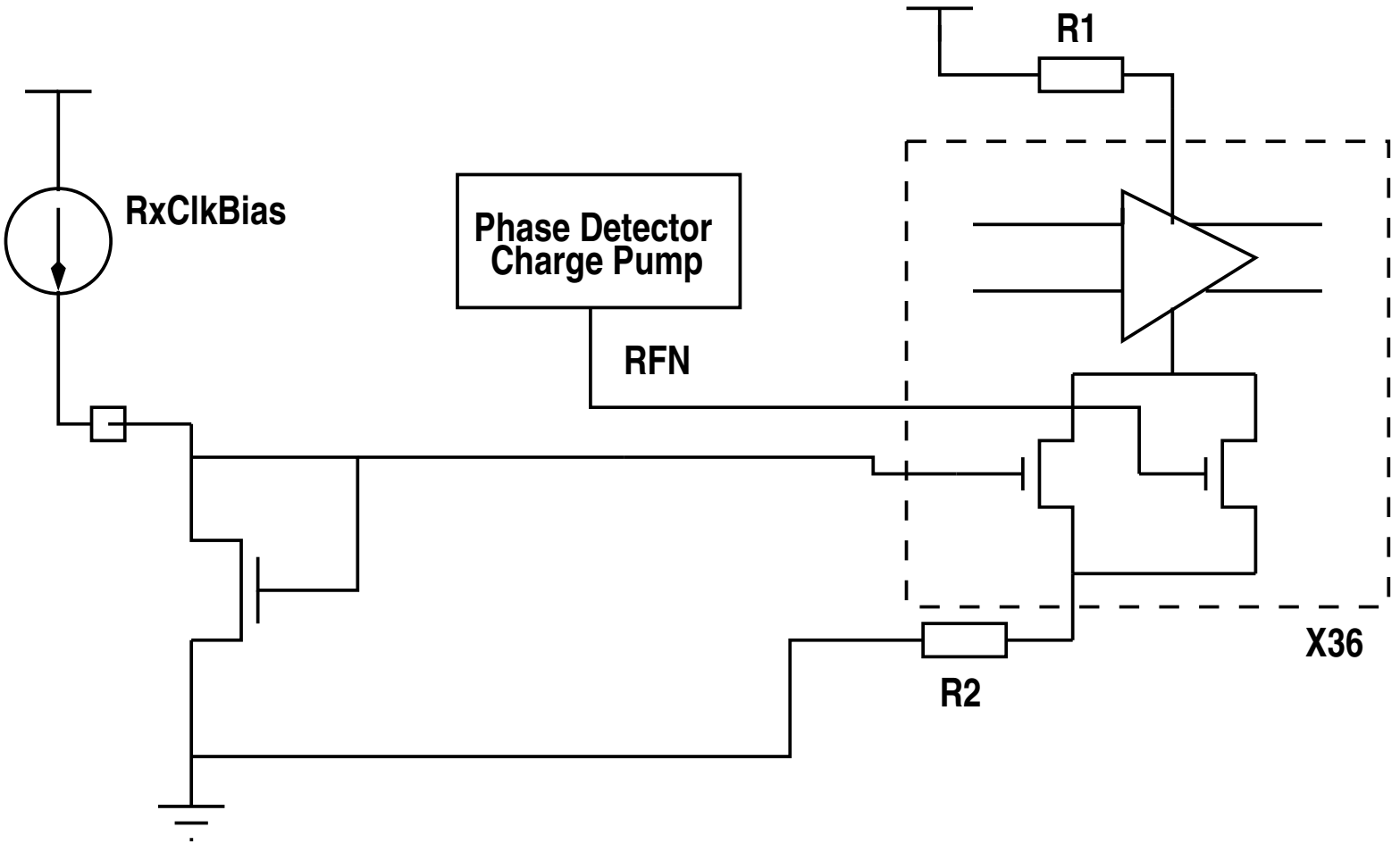
# New DLL Understanding

- DLL investigations have been successful
- Resistive paths in the power nets cause ohmic drops
  - Both VCC and GND are affected by this
  - DLL doesn't see 1.2V when powered "normally"
  - Current reference mirroring connected to different ground domains
- Experimental evidence supports simulation
  - No doubt over the issue
- Operational point optimized
  - Permits the DLL to work at full speed (320MHz)
  - and beyond (400MHz has been acheived)

# Approximate Schematic



# Current Mirroring



# Working Point

- New working point estimated
  - VDD Set to 1.5V
  - Measurements of RFN permit us to estimate:
    - GND(DL) $\approx$ 100mV
    - VDD(DL) $\approx$ 1300mV
    - Circuit draws $\approx$ 160mA
  - RxClkBias (external) 300uA
- DLL measured to lock at 320MHz
  - 200uA $\lesssim$ RxClkBias (external) $\lesssim$ 300uA

# Synopsis and Outlook

- Synopsis
  - In-depth look at the DL
    - yielded a detailed understanding of the design and operation
    - new working point found
    - gives behaviour in agreement with design and simulation
  - DLL now runs at (at least) 320MHz
    - can be operated faster for a smaller time bin
- Outlook
  - Characterisation measurements will be restarted in the new lab
  - Detailed presentation of final performance at the next meeting