Charge measurement with TDC per pixel architecture

G. Dellacasa, S. Garbolino, F. Marchetto, G. Mazza, A. Rivetti
I.N.F.N. Sezione di Torino, Via Pietro Giuria 1 Torino, 10125, Italy

Basic Facts (1)

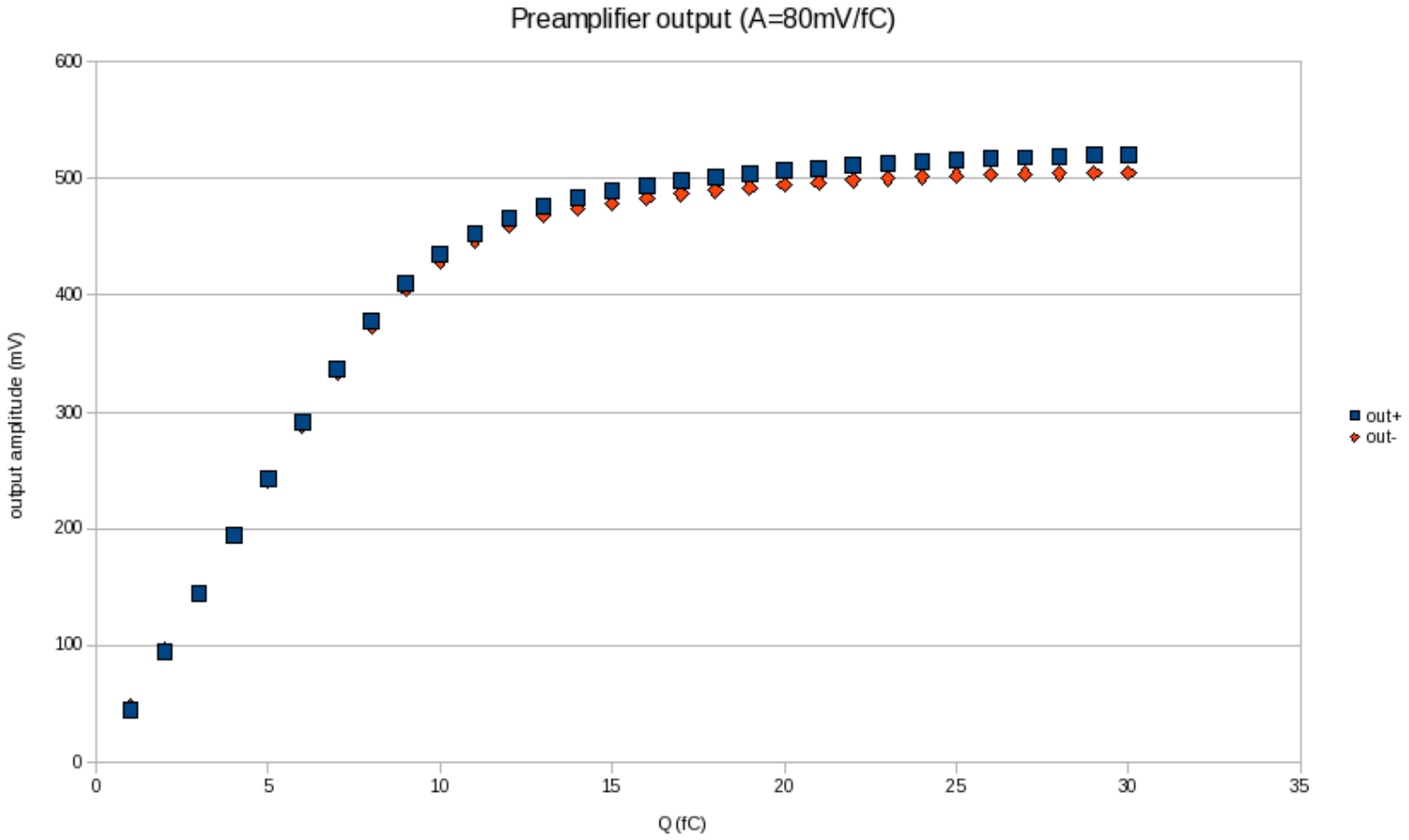
Assuming 200 μm thick silicon (1 mip = 2.4 fC):

the fraction of particles releasing more than 4 mips is 9×10^{-3}
the fraction of particles releasing more than 5 mips is 6.1×10^{-3}

Where the threshold?
If a threshold higher than 5 mips is required, at which signal it should be applied?

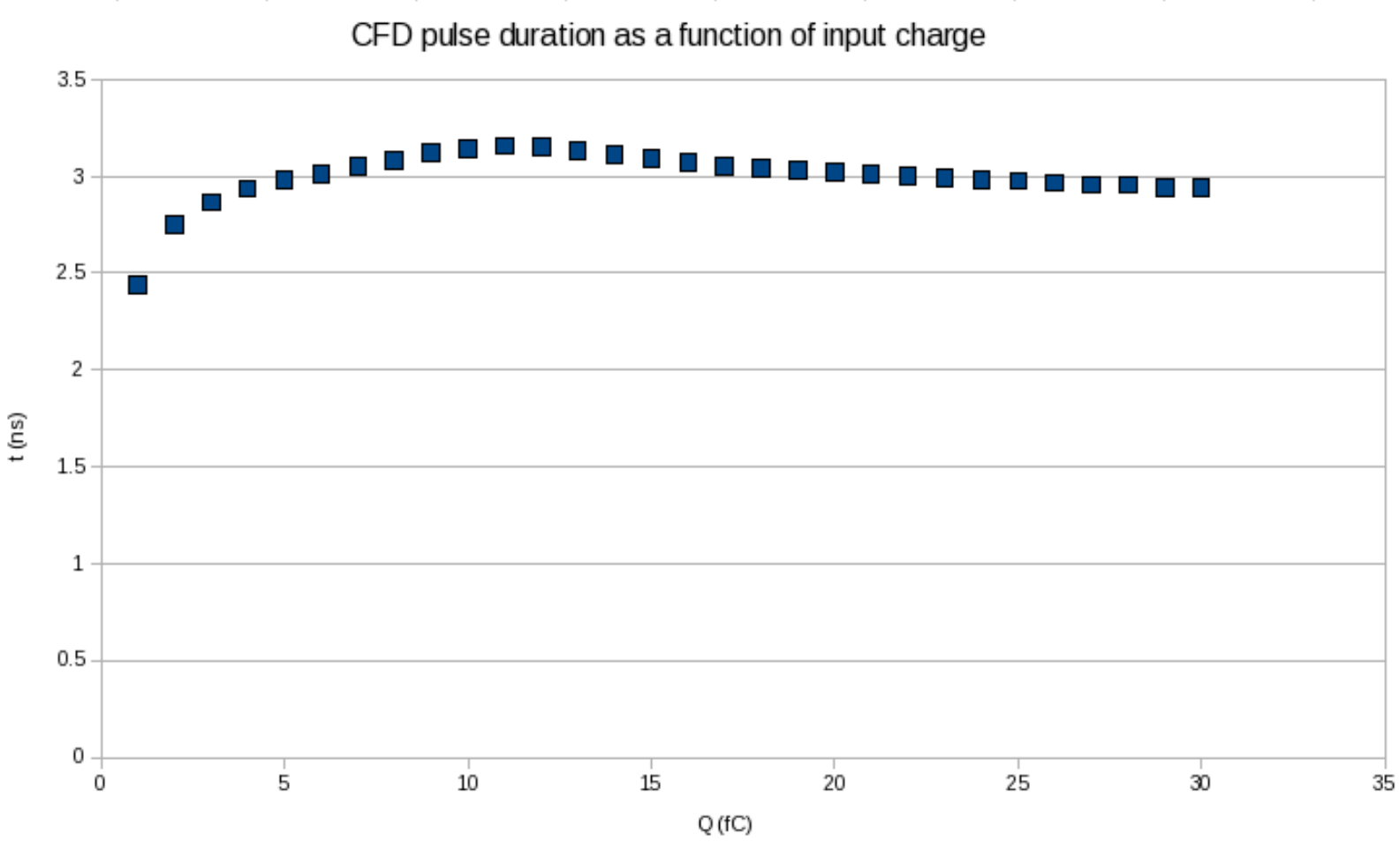
Basic Facts (2)

The information should be extracted at the front-end amplifier, which gain has been set to saturate at 10 fC



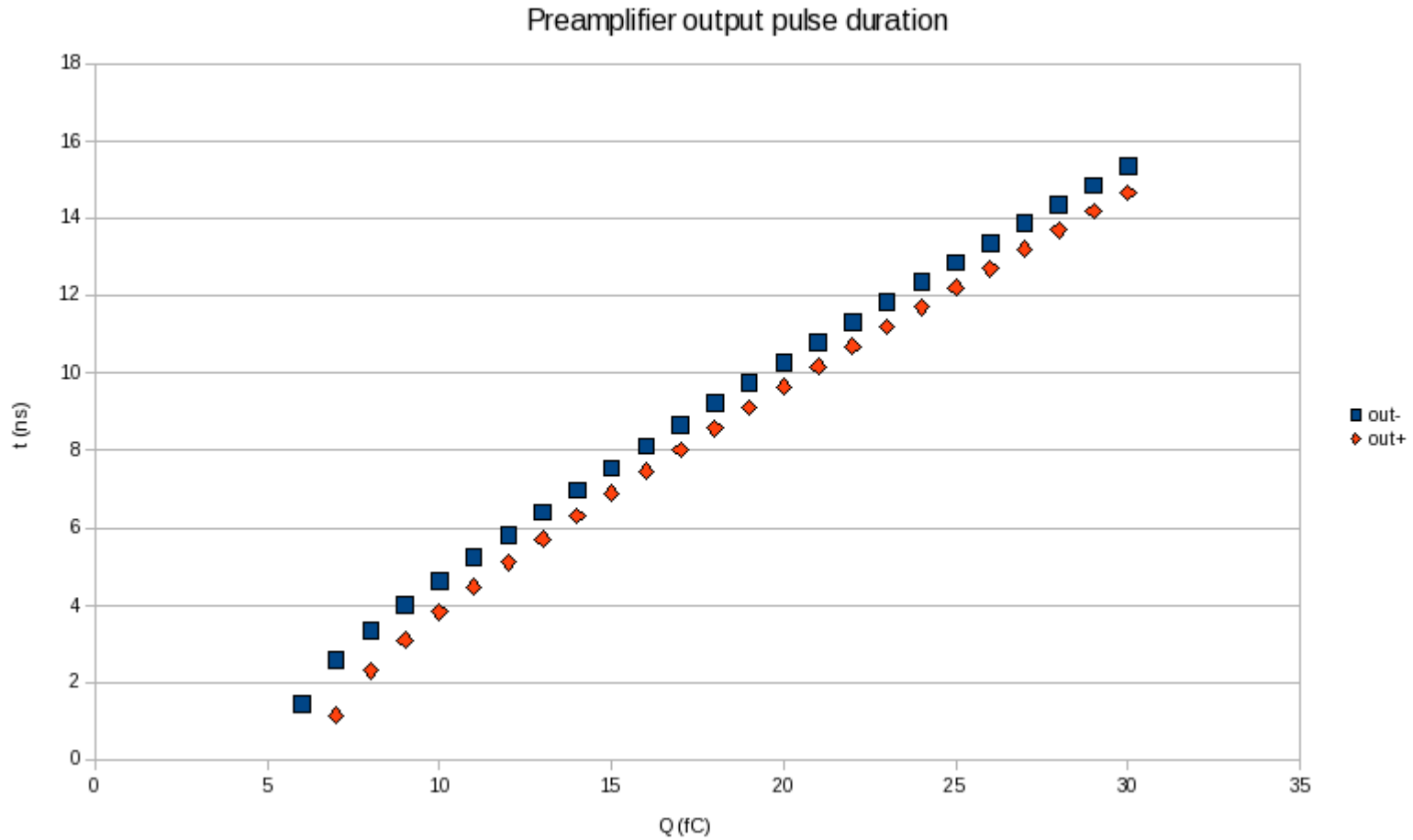
Basic Facts (3)

In the TDC per pixel architecture the duration of the CFD pulse is not proportional to the input charge

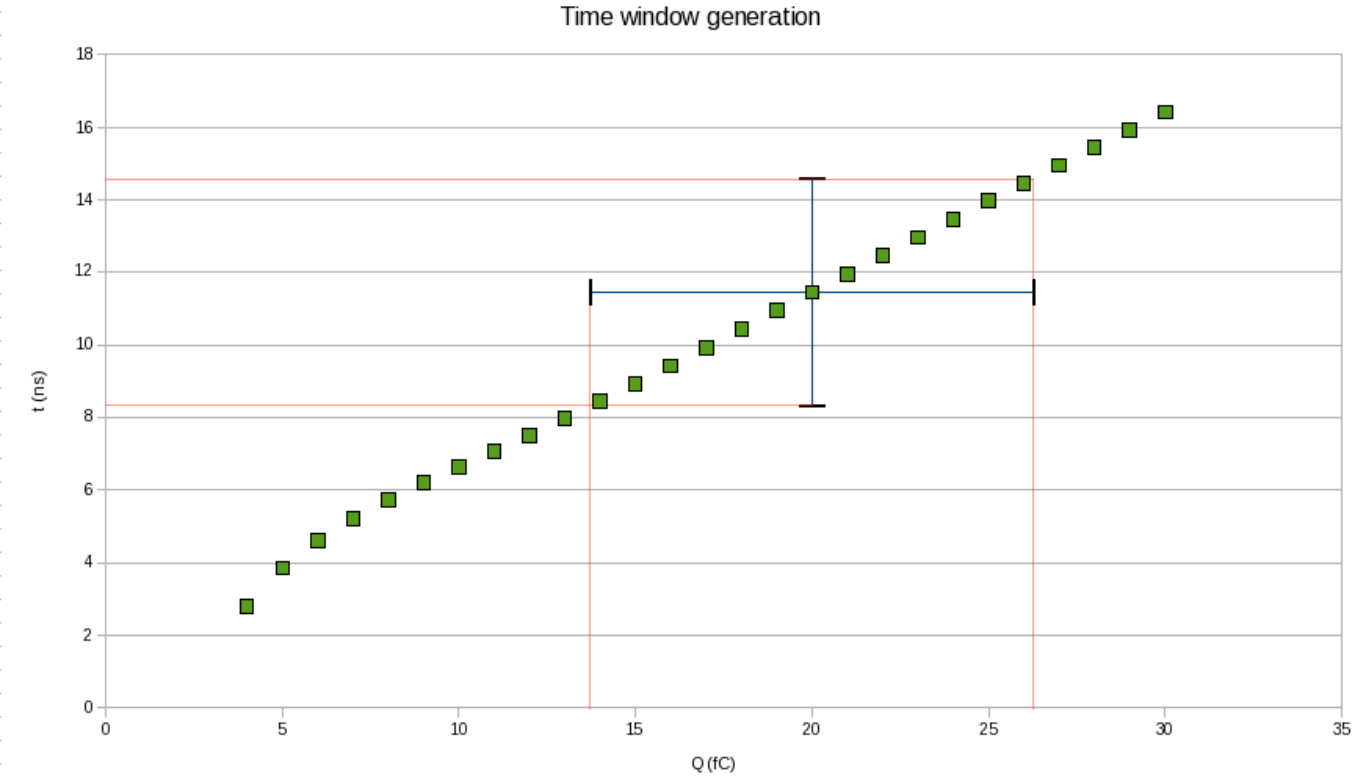


Basic Facts (4)

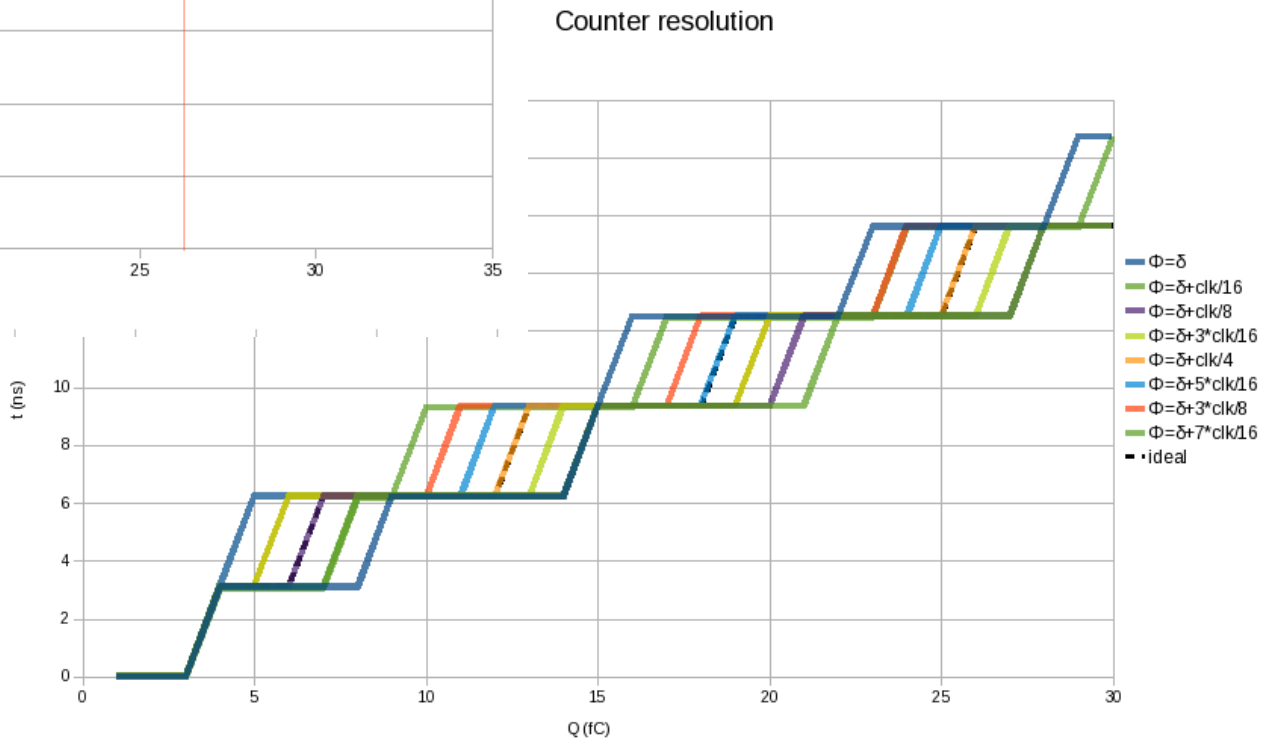
The duration of preamplifier pulse is proportional to the input charge



Two possible solutions: simple TOT



Preamplifier + leading edge comparator+ 3 bit counter: not enough to get rid of CFD for timing information, but it provides more levels of charge discrimination

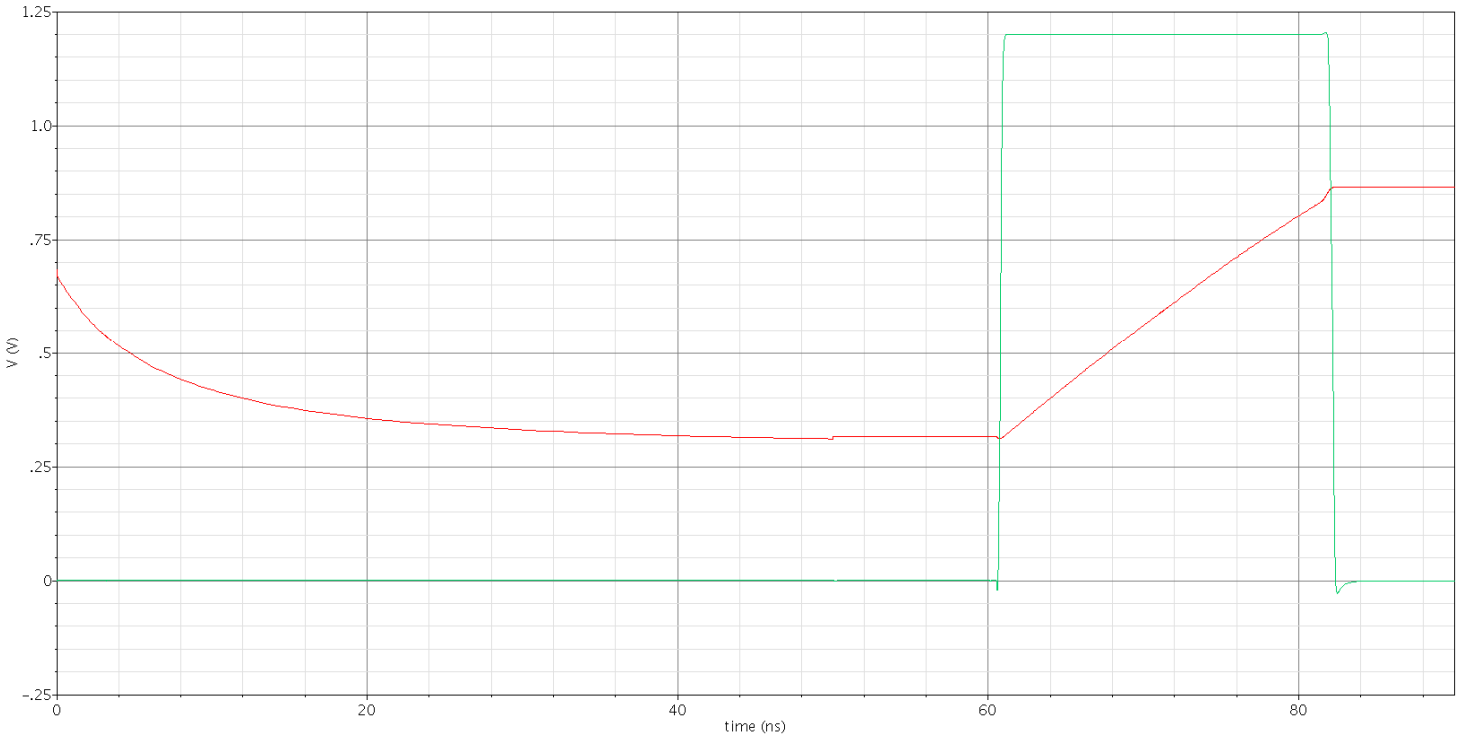


dQ/dt = 2 fC/ns
dt = 3.125ns → dQ = 6.25fC

if $t = t_0 \pm 3.125$ns
than $Q = Q_0 \pm 6.25$fC

Two possible solutions: simple TDC (1)

Preamplifier + leading edge comparator + simple TAC + two or more threshold comparators



dQ/dt = 2 fC/ns
dV/dt = 30 mV/ns

→ dV/dQ = 15 mV/fC

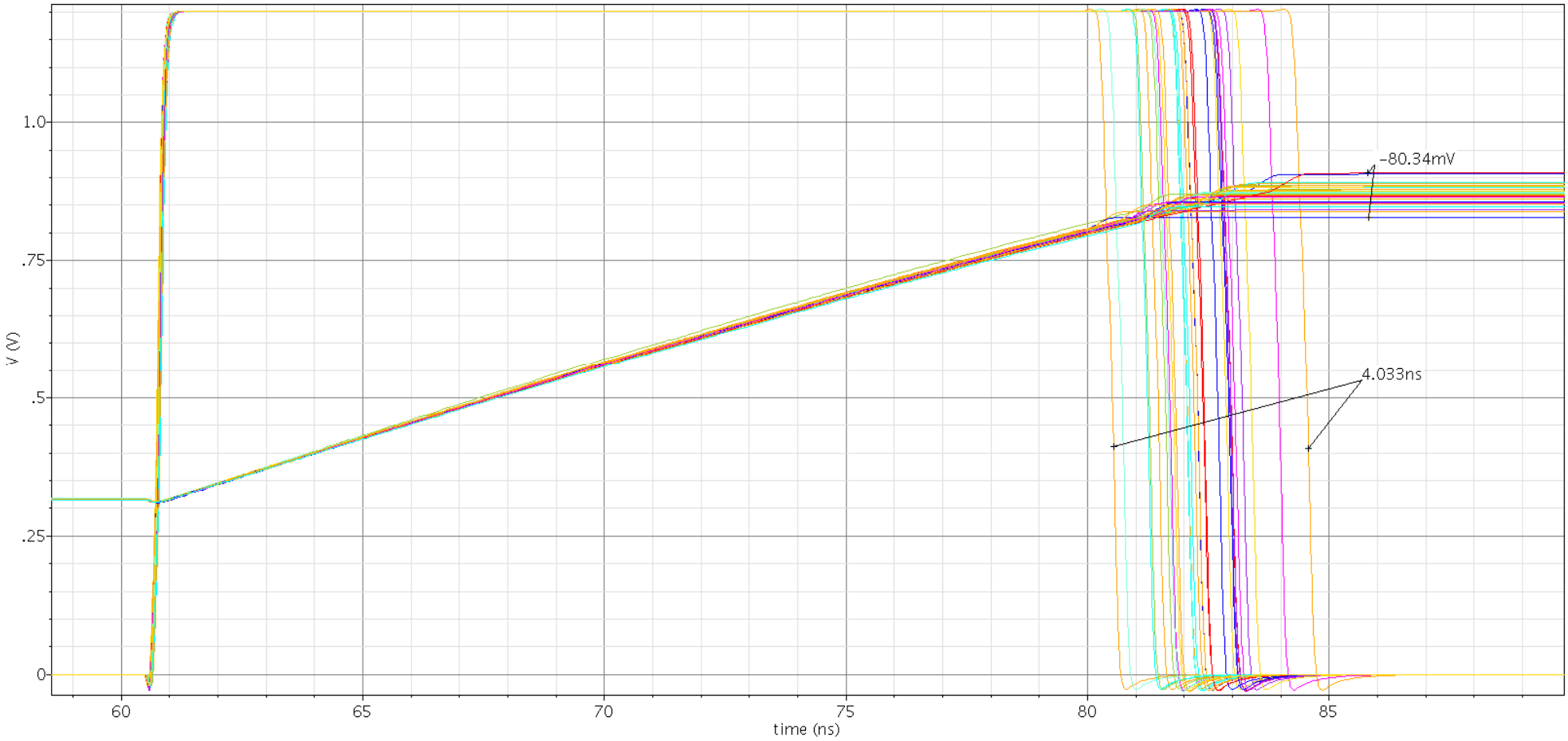
If Q_{th1} = (5 ± 1) mips
Q_{th2} = (10 ± 1) mips

than V_{th1} = (480 ± 36) mV
V_{th2} = (660 ± 36) mV

Two possible solutions: simple TDC (2)

The spread due to the mismatch is mainly introduced by the variation of time window length: optimization

The spread due to the process can be removed introducing a calibration per column of pixel



Summary

- Simple TOT solution seems to have a bad resolution which doesn't allow to apply two thresholds
- Simple TDC solution so far seems to work:
  - Its performance can be improveded by optimization
  - In future a design using synchronous comparators with latches will reduce power dissipation (<100μW) and allow the introduction of offset compensation methods → more than two thresholds if needed