Status Report of TDC-per Pixel Chip Test

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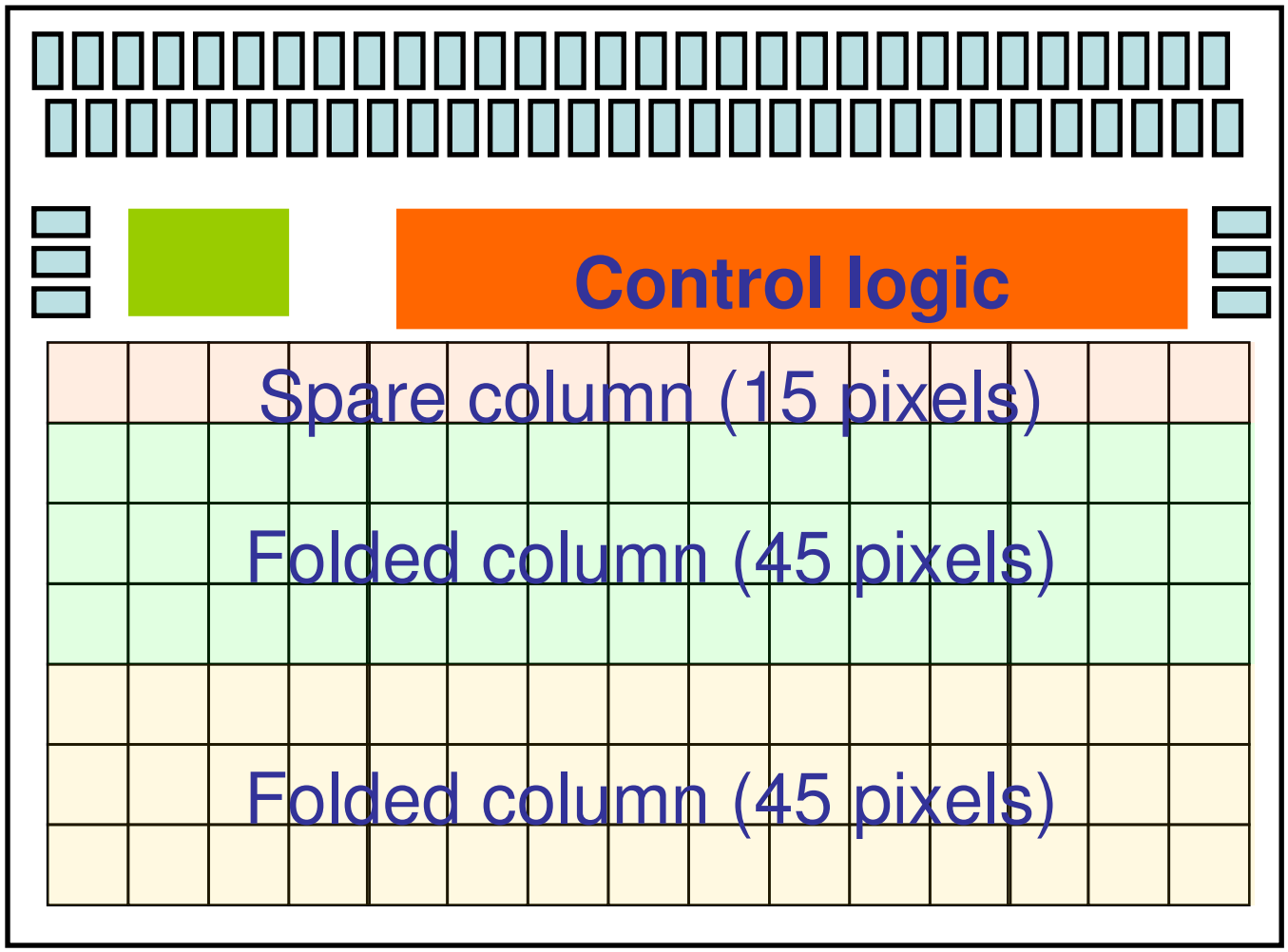
Demonstrator Chip



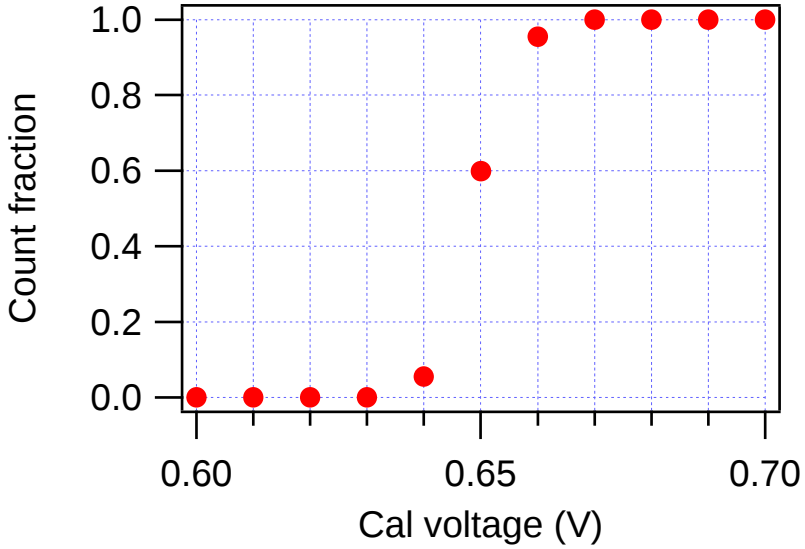
- One column with 15 pixels and two folded columns with 45 pixels
- Two pixels for analog test

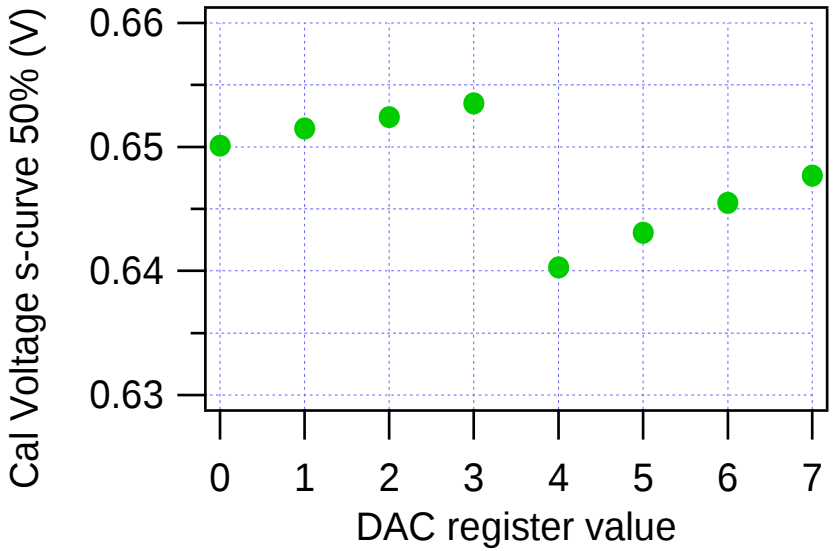
Test set-up

- FPGA software under development
- Tests are made using the oscilloscope and the Logic State Analyzer (LSA) together with Labview routines developed by Richard Wheadon
- Matrix calibration and time measurements underway

Pixel matrix measurements

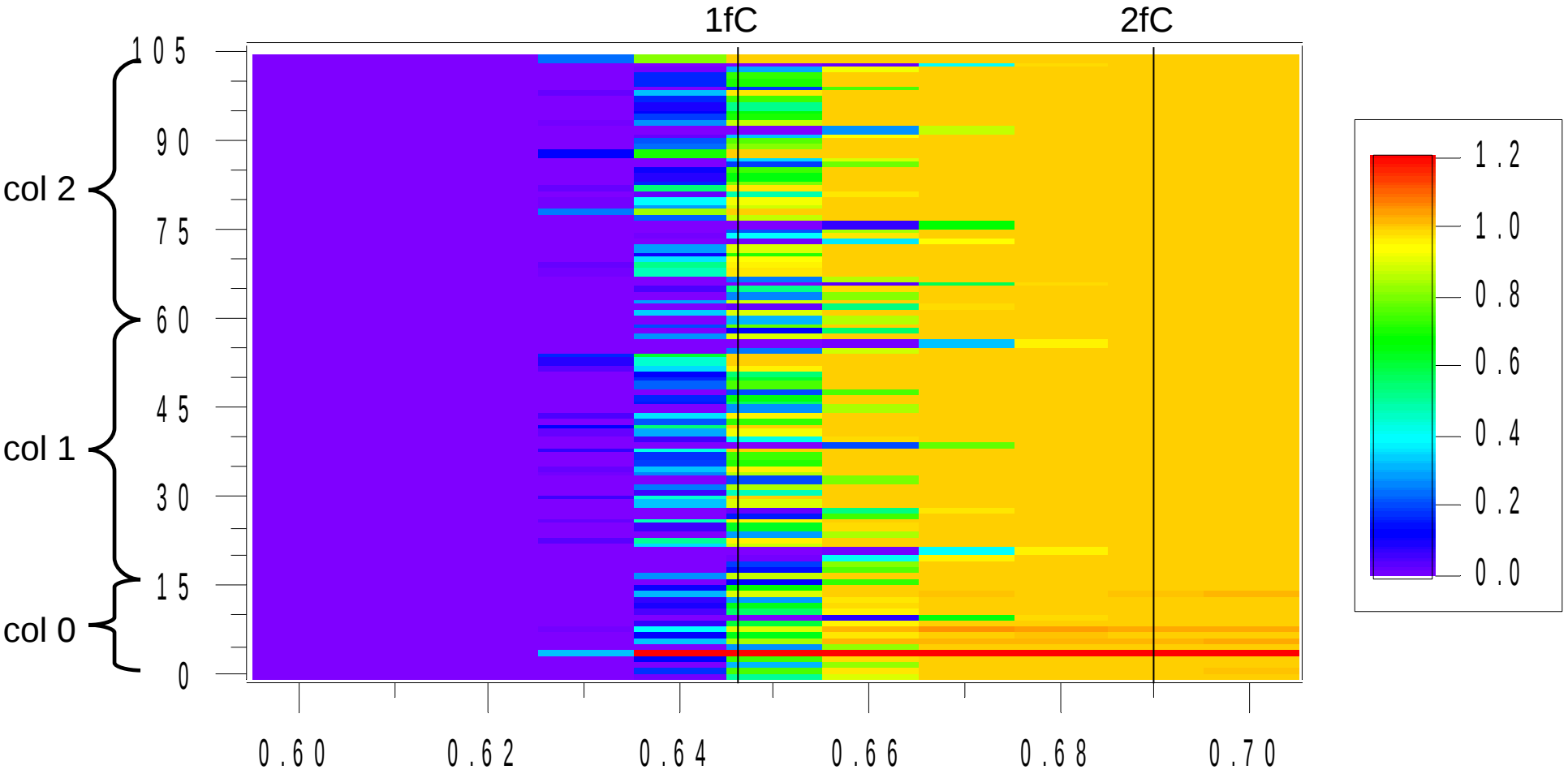
- Feed through of a digital signal: it was necessary to slow down the preamp





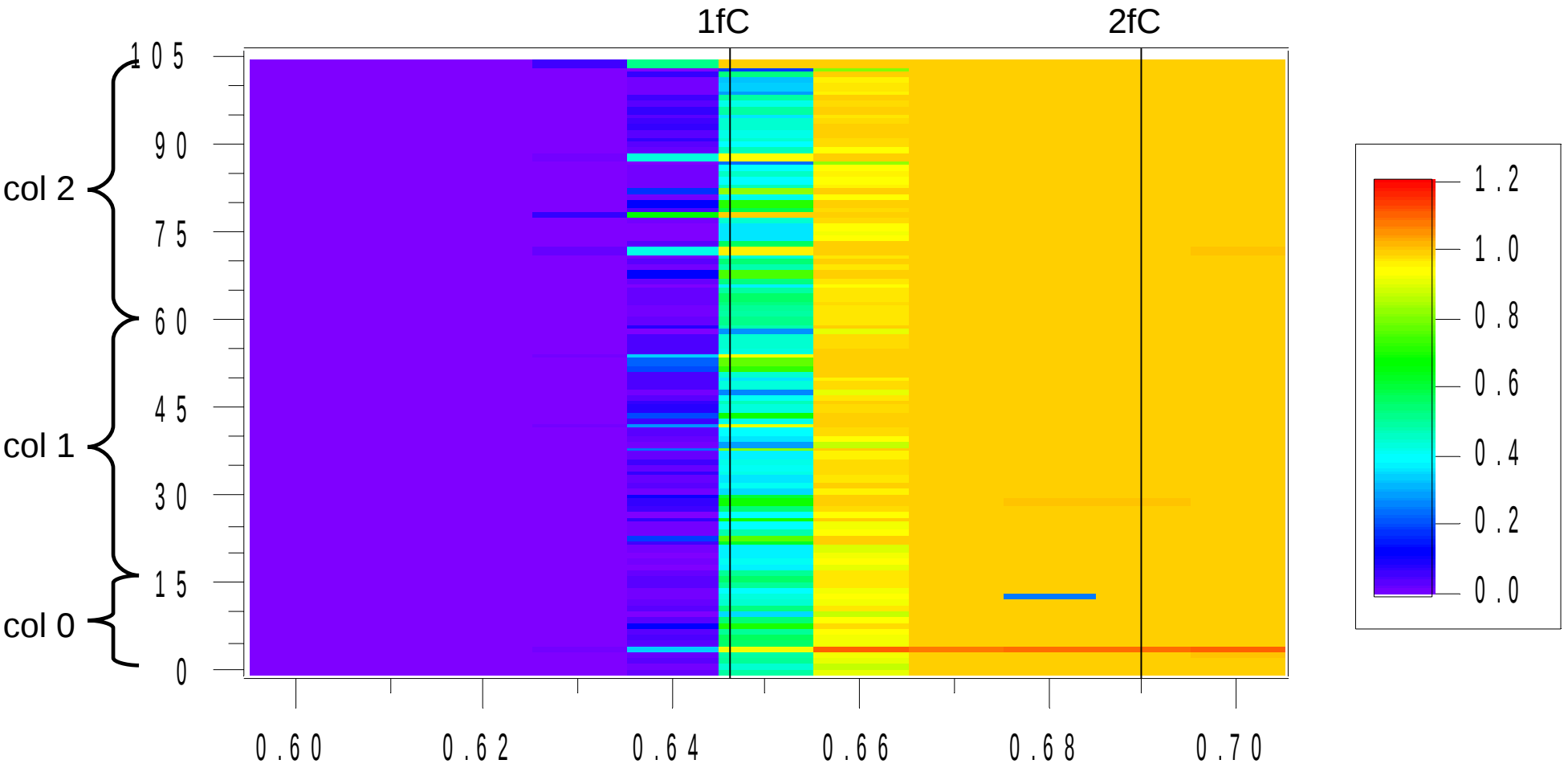
Efficiency (1)

- A full scan was performed to equalize the channels of the matrix at 1.2V



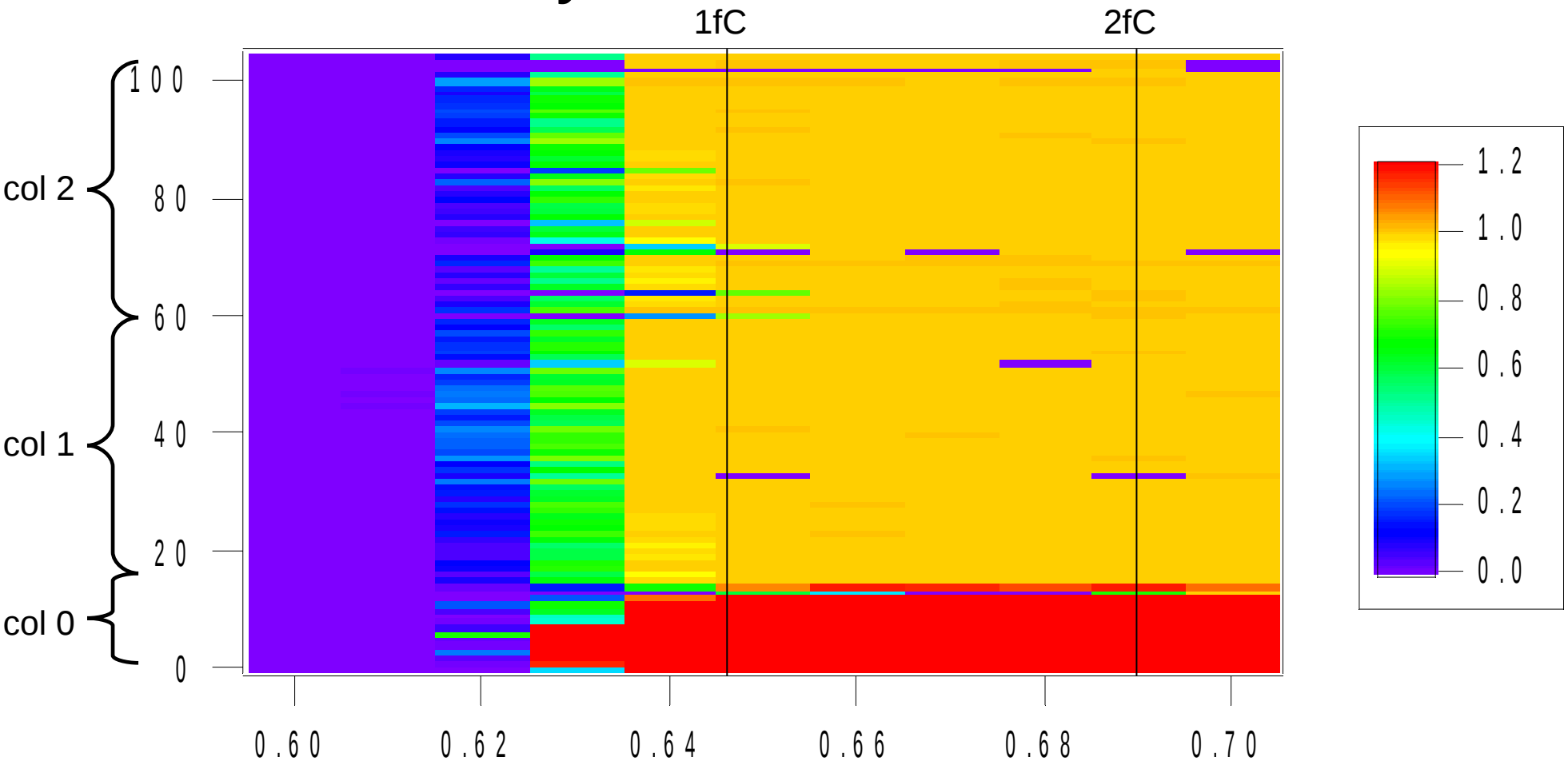
Efficiency (2)

- First equalization: full efficiency at 1.45fC



Efficiency (3)

- Second equalization: full efficiency at 1fC, but column 0 noisy

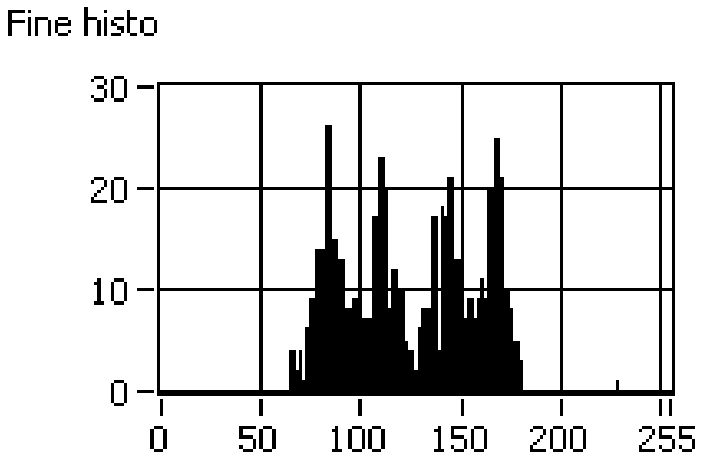


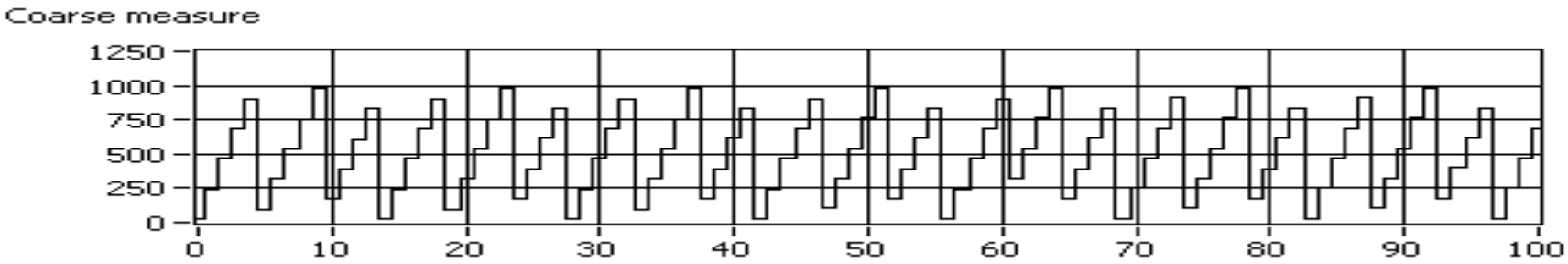
Next step

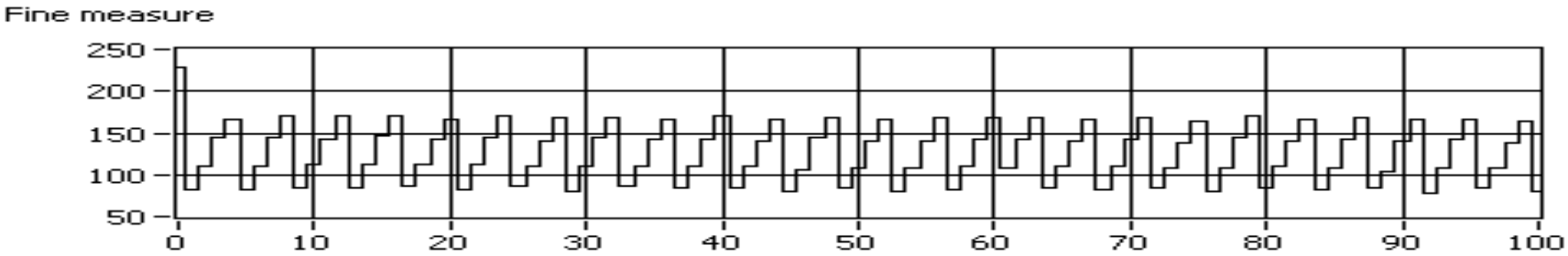
- Set-up for time measurement using LSA and Labview acquisition software
- Working at 1.5V and 128MHz because of a problem with the EoC signal due to an under-sized buffer

Preliminary time measure (1)

- Asynchronous Test Pulse with period of 50µs





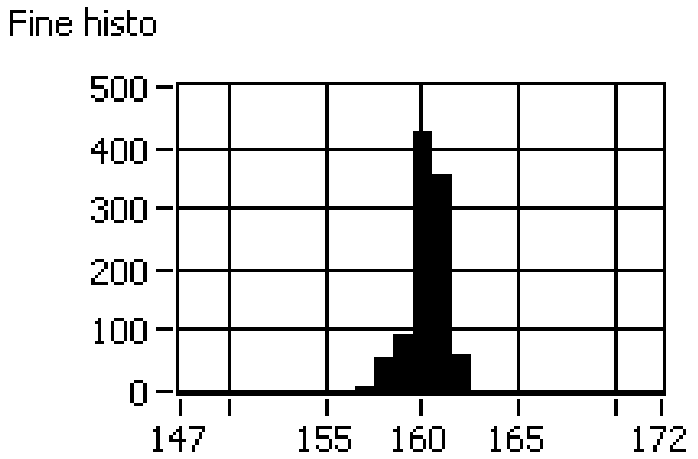


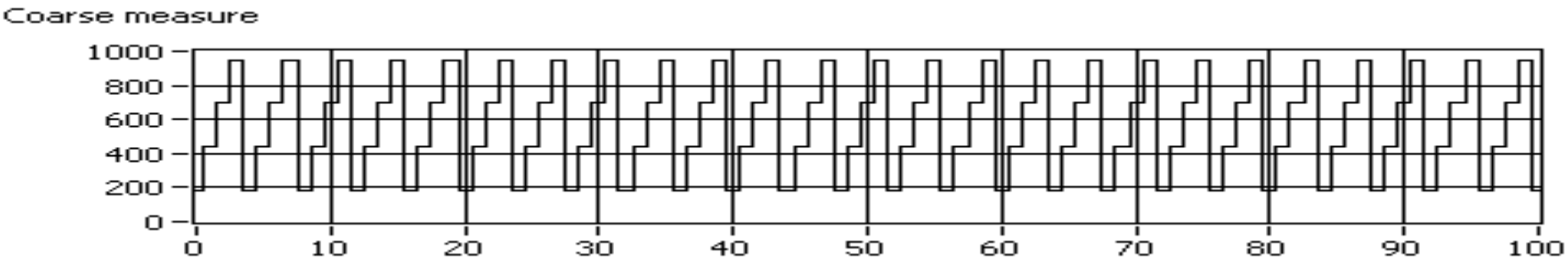
Preliminary time measures (2)

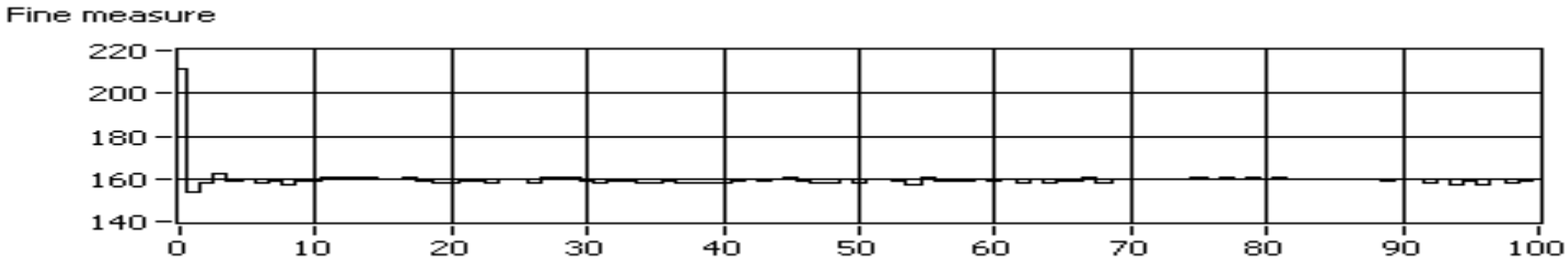
- Synchronous Test Pulse

  jitter at 2fC: 160ps (rms)

  jitter at 6fC: 120ps (rms)







Summary and Outlook

- Good efficiency on pixel matrix was obtained at 1.2V
- First data from the matrix make sense
- Calibration of TDC and new equalization at 1.5V required before starting acquiring data