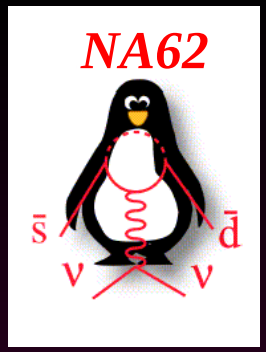

NA62 - GTK

Sezione di Torino

CFD/TAC based GTK readout architecture : design considerations and test results

S. Chiozzi, G. Dellacasa, S. Garbolino, F. Marchetto
S. Martoiu, G. Mazza, A. Rivetti, R. Wheadon

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Motivations

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- CFD inherently time-walk free (at 1st order)
  - no need of calibration
  - no need of extra data
- TAC based TDC can be integrated in the pixel area
  - only one time critical signal (clock)
  - each pixel operates independently
  - takes advantage of the relatively large pixel area

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CFD-TAC scheme

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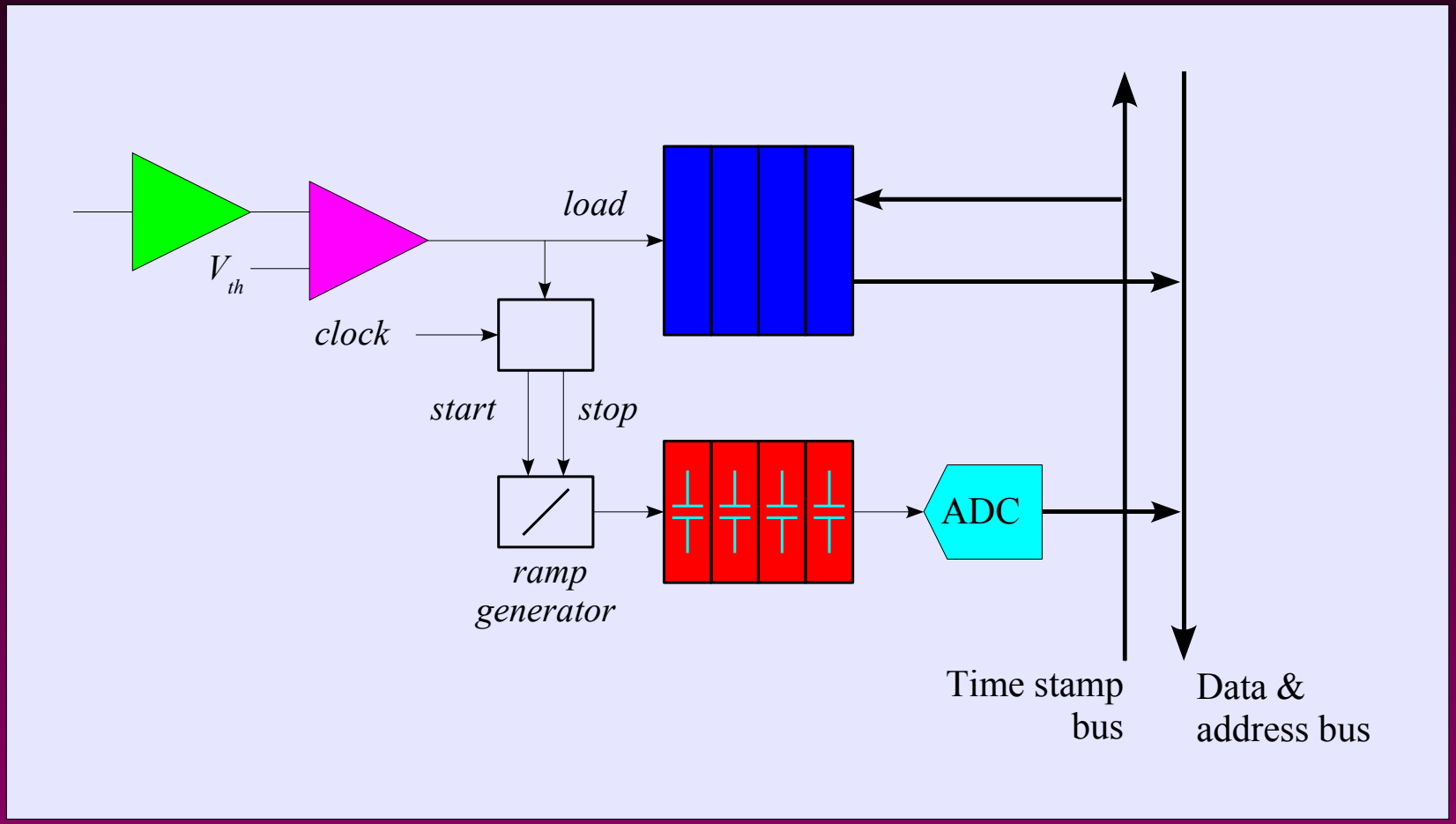
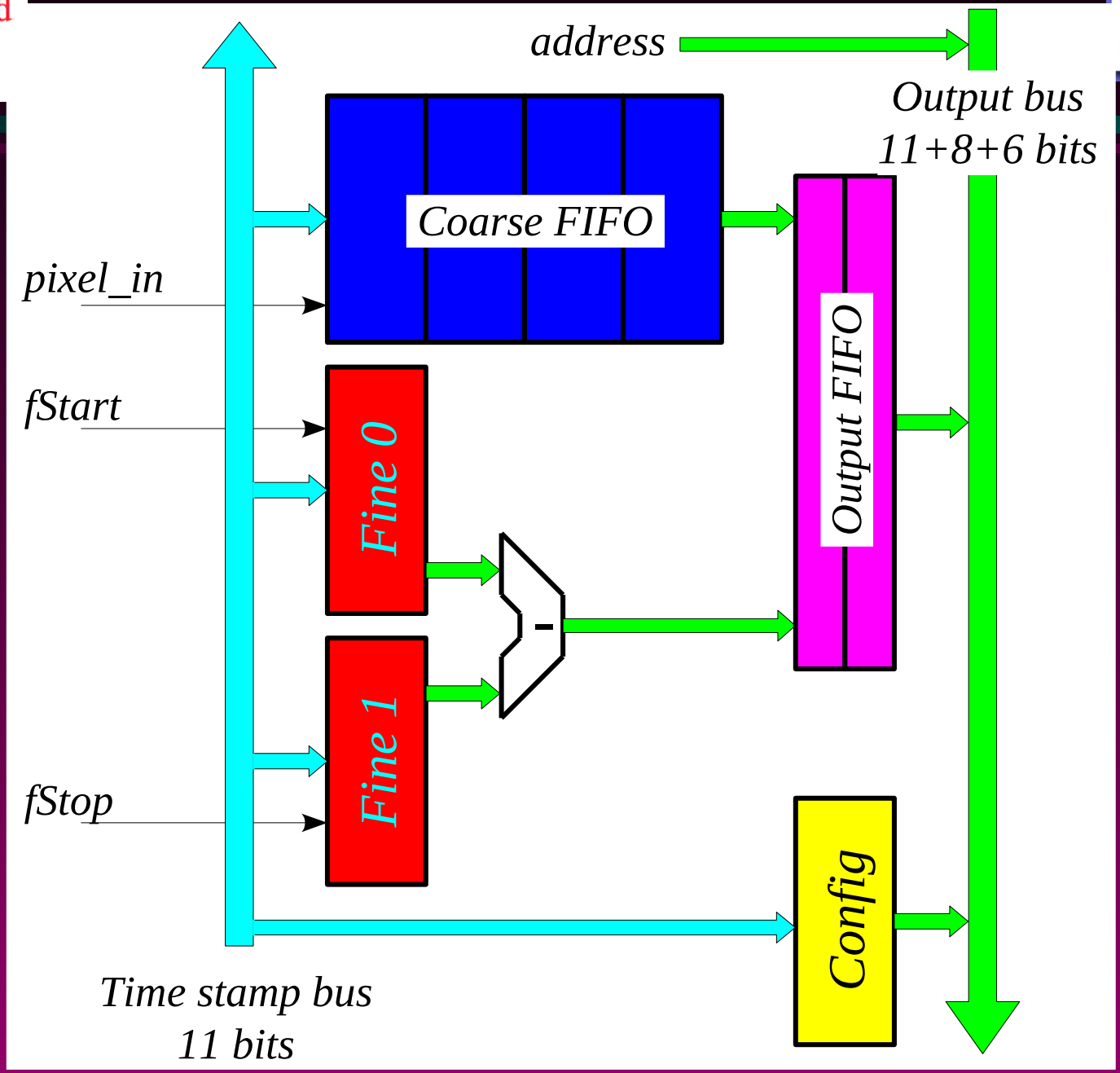


Data conversion



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Multi-buffer scheme

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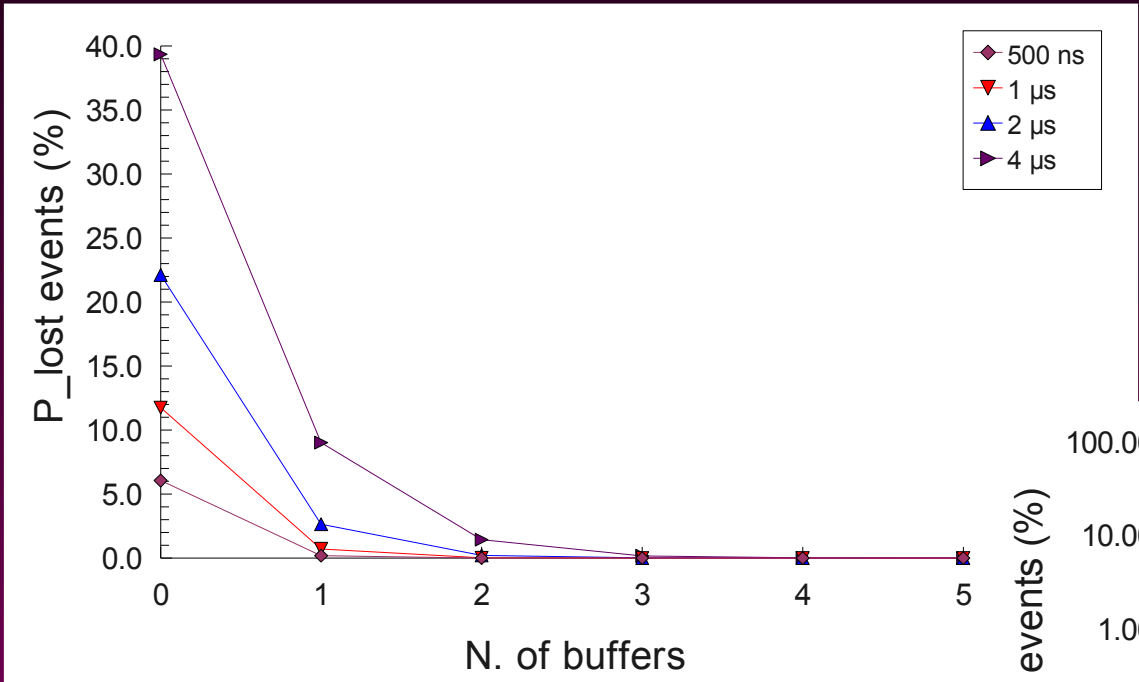

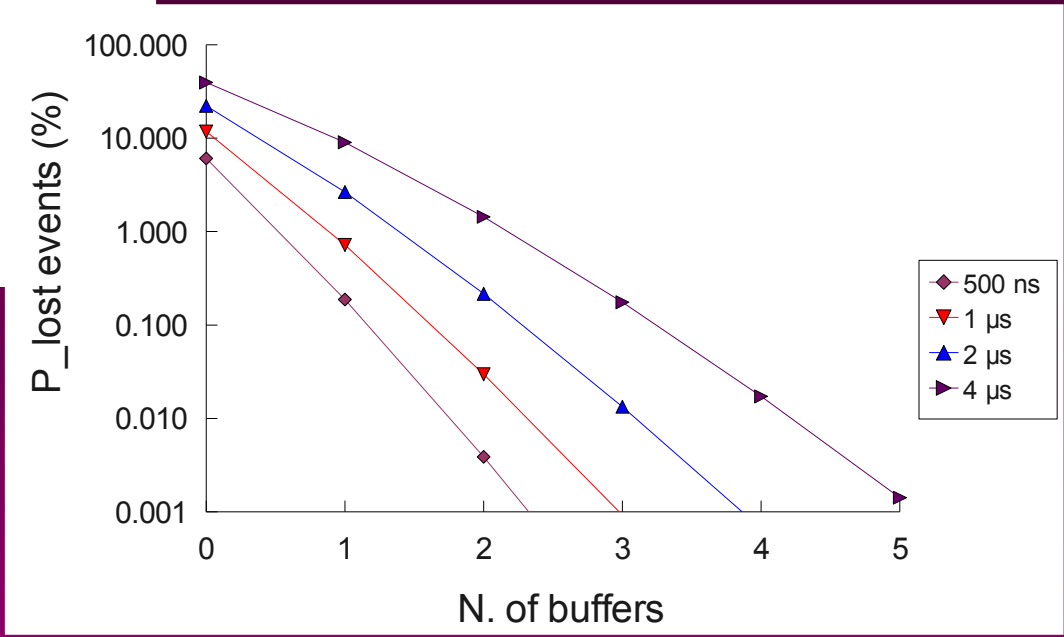

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Prototype layout

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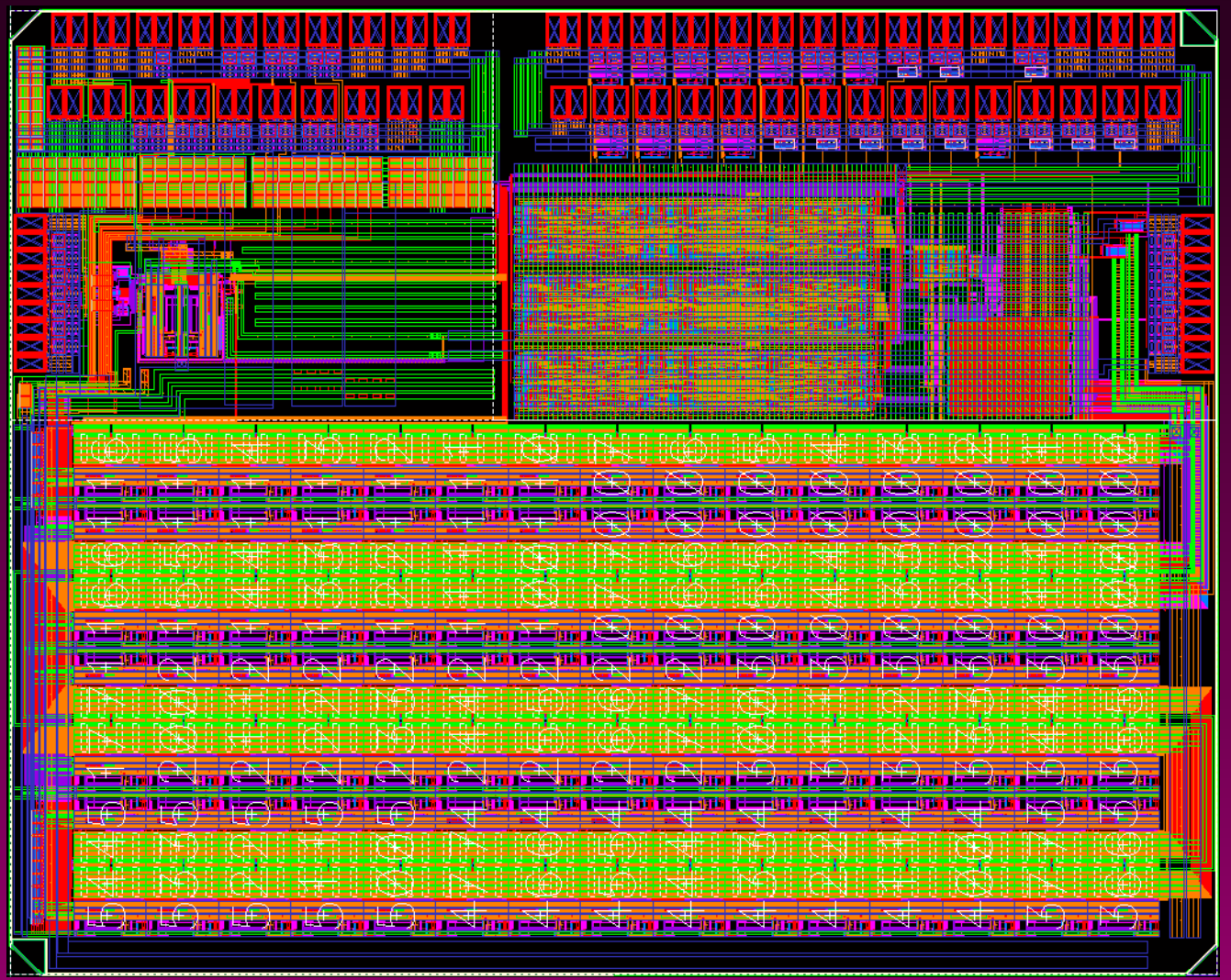
- CMOS 0.13 μm
- 5 mm × 4 mm
- 118 bonding wire pads
- 106 bump bonding pads
- 105+2 pixel cells
- LVDS interface
- 1.5 V core power supply
- 2.5 V periphery power supply



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Layout details

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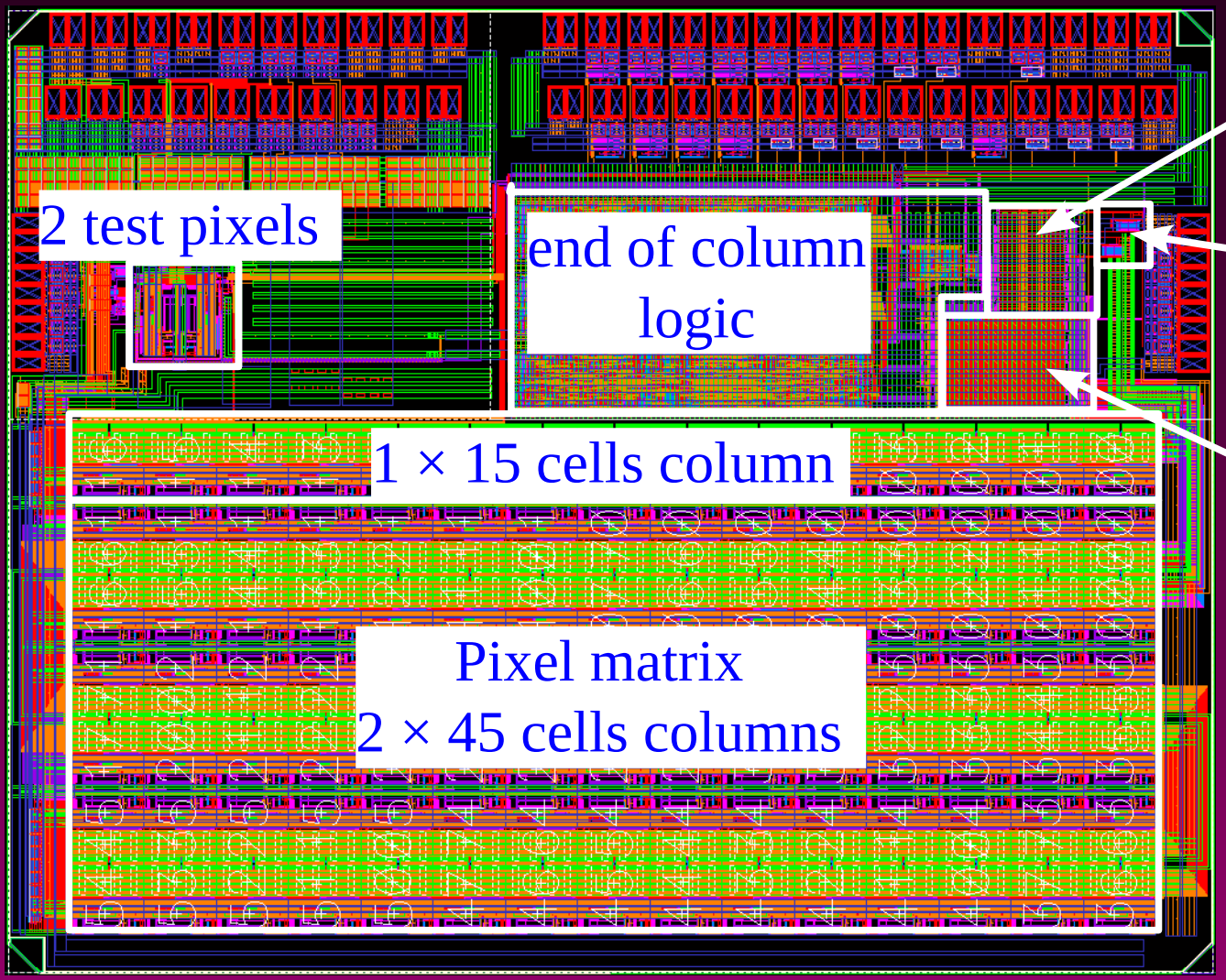

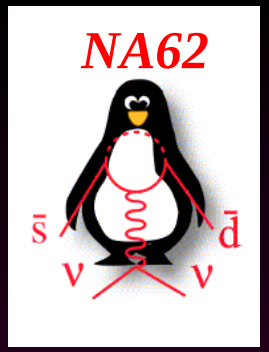

Pixel matrix

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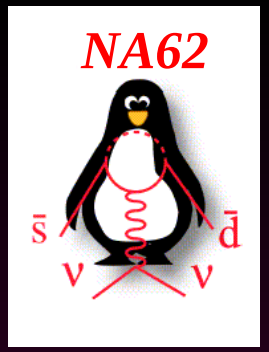
- 7 × 15 cells matrix
- Two 45 cells columns + one 15 cells column
- Folded layout to save space
- Clock and calibration signals distributed over a transmission line
- Time stamp and command distributed over pseudo differential CMOS lines



Pixel cell - analogue

Sezione di Torino

- Fully differential preamplifier and CFD
- 3 bit DAC for threshold control
- 3 bit DAC for TDC discharge current control
- Test mode selection :
  - Charge injection via a 22.1 fF capacitor
  - TAC test signal
- Externally accessible comparator and TAC window output

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Pixel cell - digital

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- Four 11 bits registers coarse buffer
- Two 19 bits registers output buffer
- Directly addressable 8 bits configuration register
- Hamming encoding for registers and FSMs
- Separate error signals for SEU in the registers and FSMs

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Column Rx/Tx

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- Pseudo differential CMOS driver with reduced voltage swing and pre-emphasis
- Sense amplifier based cells readout with a three phases readout cycle (two clock cycles)
- Differential current clock drivers over a 100 Ω transmission line
- token, busy, old_data and SEU_error signals are propagated via an OR chain

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Column controller

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- Hamming protected 2×24×32 data FIFO and 1×32×32 output FIFO plus control logic
- Two differential outputs per column : serial data out and data valid
- Data transmission can be set to f_{CK}, $f_{CK}/2$, $f_{CK}/4$ or $f_{CK}/8$.
- The counter can work either in binary or Gray encoding

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Global configuration

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- A 32 bits Chip Configuration Register is used to upload configuration informations
- A shift register is used to upload/download the configuration data.
- Bit mapping :
  - 31:29 : local configuration and driver control
  - 28:26 : not used
  - 24:11 : pixel analogue section settings
  - 10:0 : digital end of column settings

Local configuration

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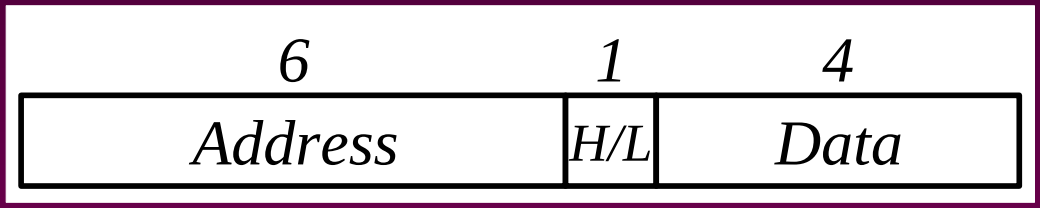
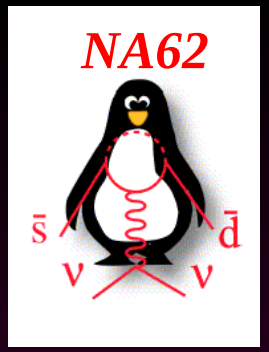
- The 8 bit pixel configuration register is accessible via the time stamp bus and the config_mode signal
- Each pixel can be independently addressed :



- The time stamp bus is externally accessible in configuration mode via a shift register



Test results

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Test setup status :

- DP+LSA test setup ok
- DG2020 calibration ongoing
- FPGA-based DAQ under development (Ferrara)
- Beta version available

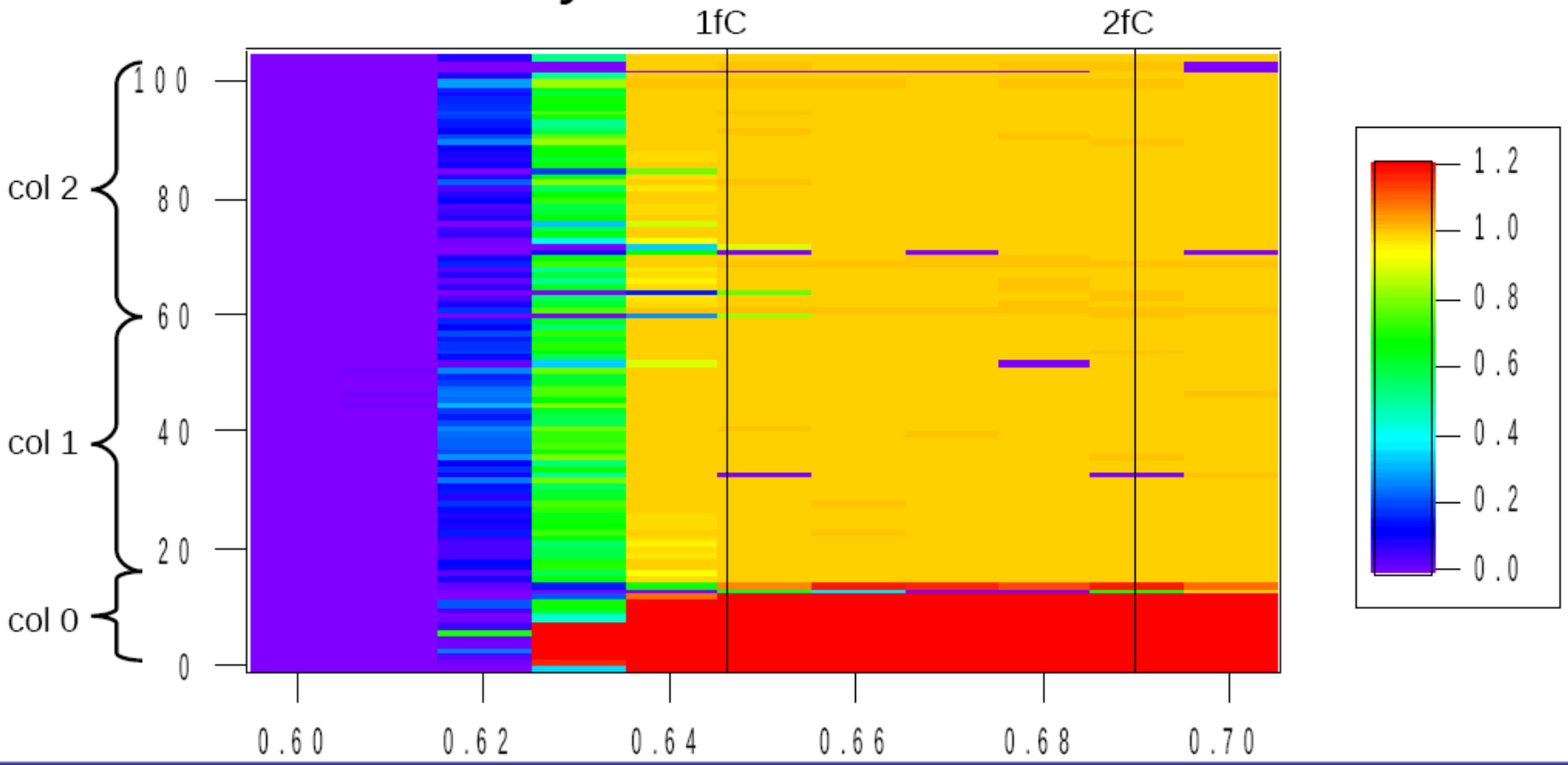
Test status :

- Pixel equalization done
- Efficiency and jitter measurement done
- TDC linearity to be done

Efficiency - 1

Sezione di Torino

- Second equalization: full efficiency at 1fC, but column 0 noisy



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Efficiency - 2

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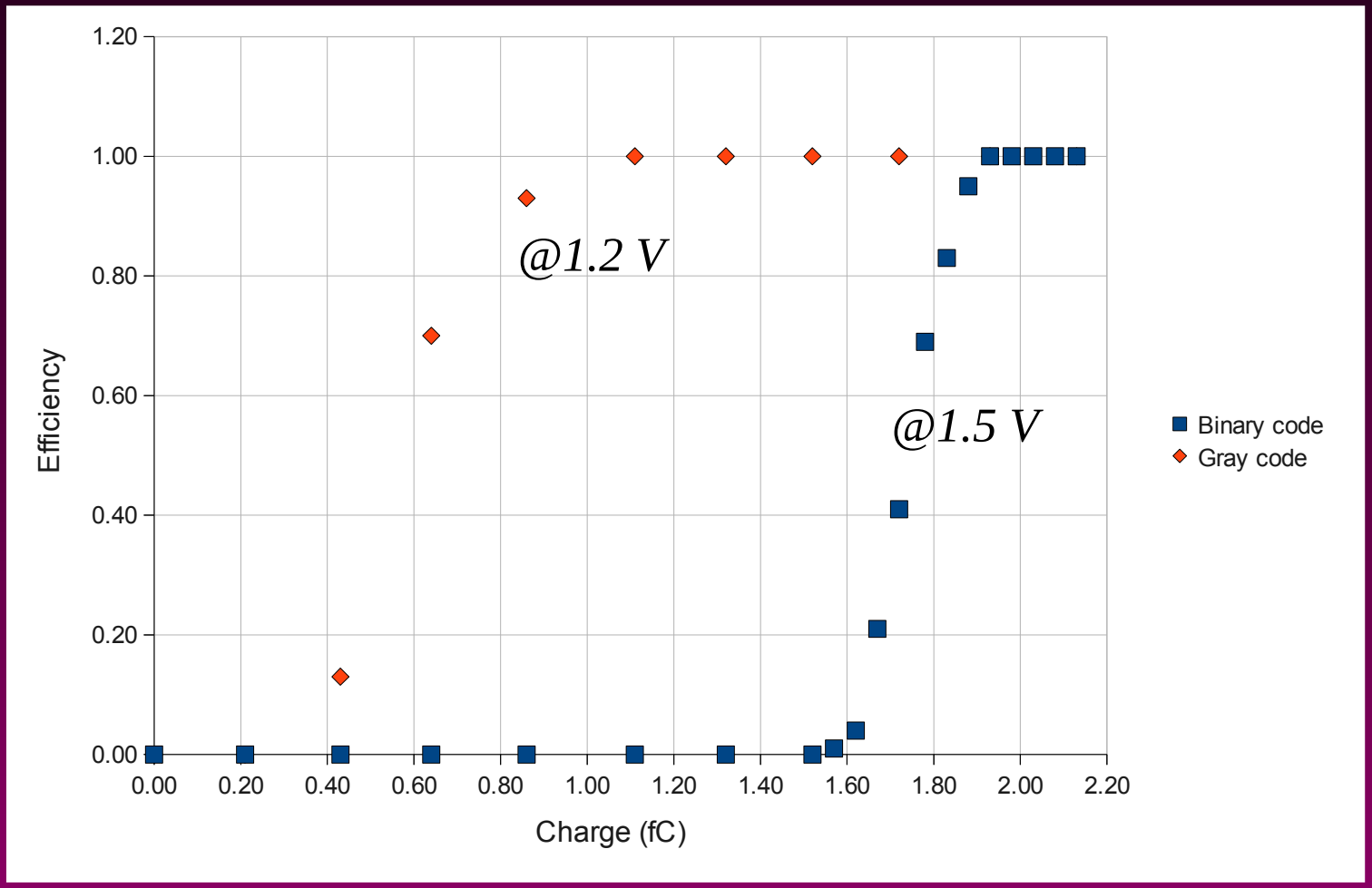

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Jitter

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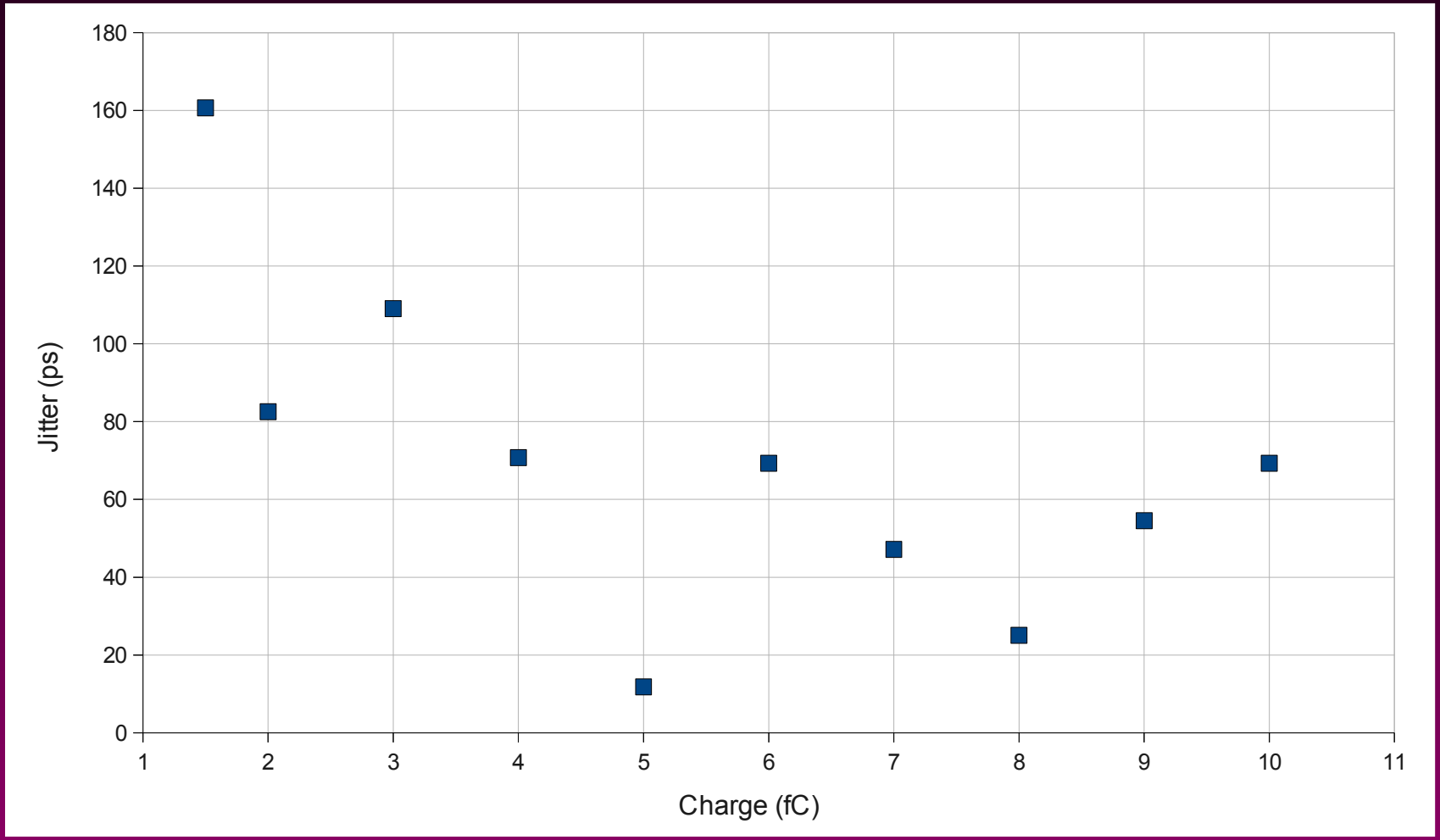
Sezione di Torino



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Time bin spread

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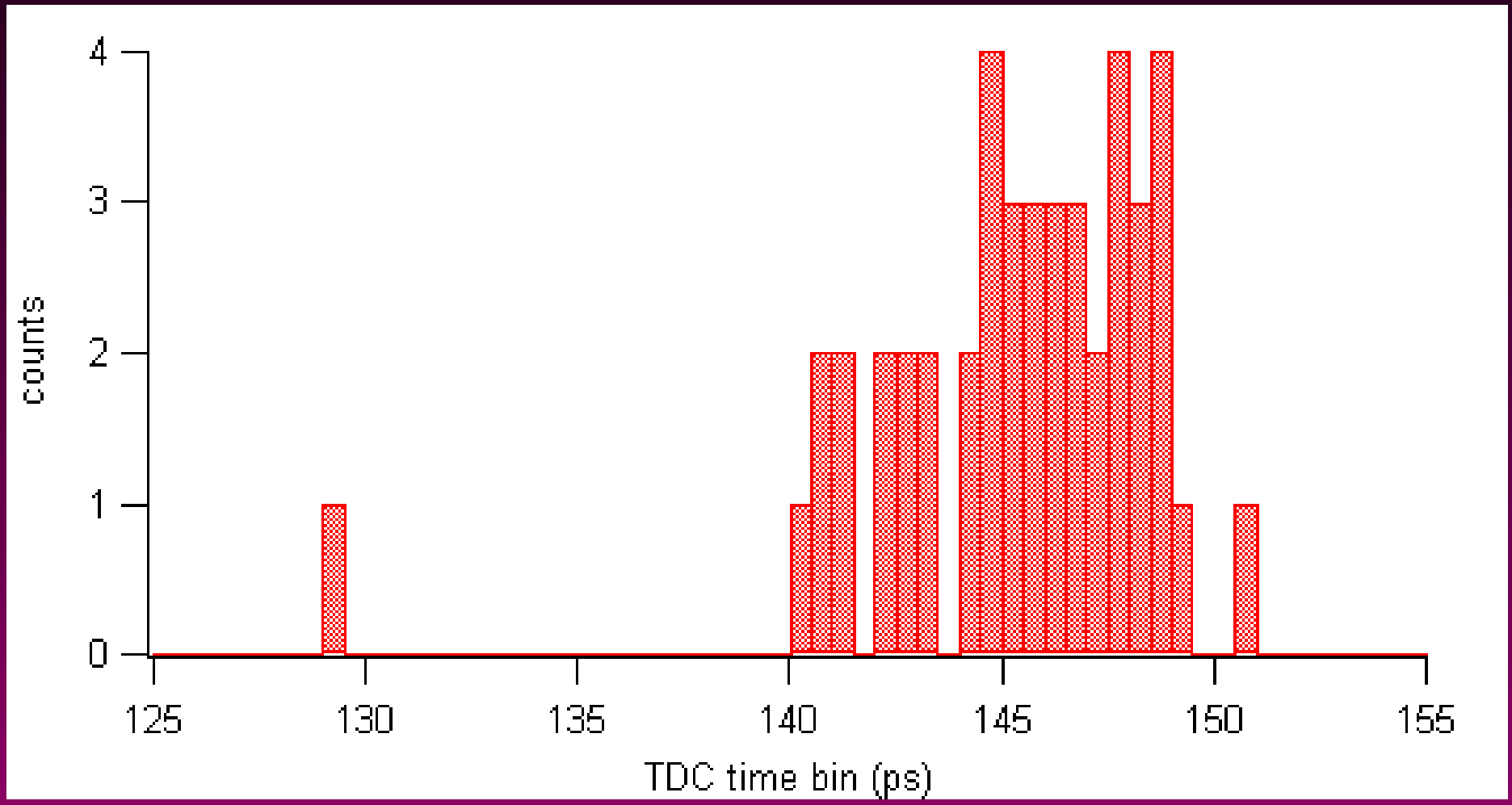

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TDC noise

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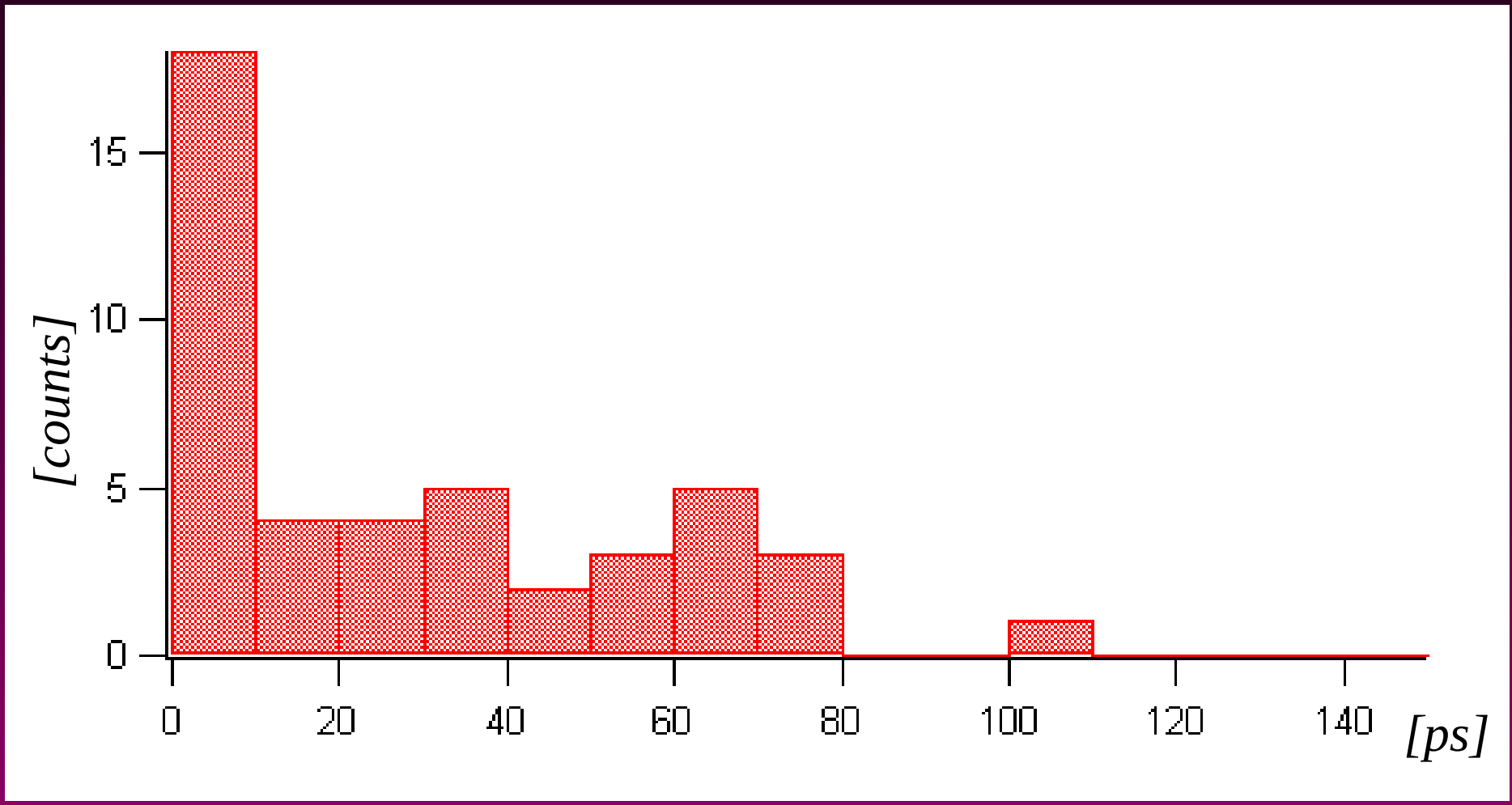
Sezione di Torino



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TDC linearity

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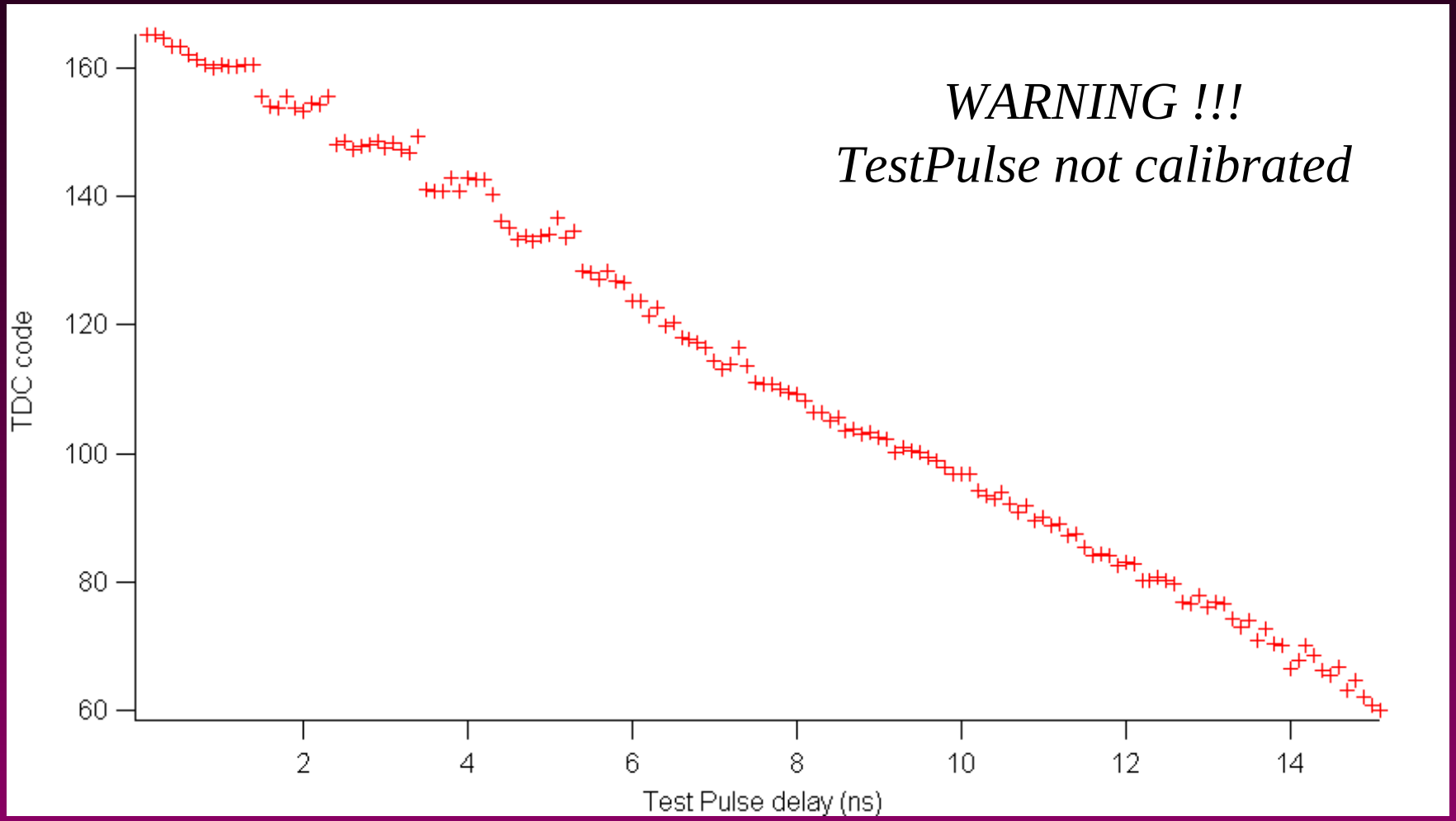

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Hiccups...

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1. CFD output not correctly connected
   - Problem can be mitigated but not fully corrected.
   - CFD performances can be studied separately
2. Digital logic output driver undersized
   - Working frequency limited at 128 MHz @1.5 V
   - Time bin still in specs
3. Incorrect subtraction in Gray mode
   - Some data processing required to get the info
   - Some data to be discarded ?

Time walk patch

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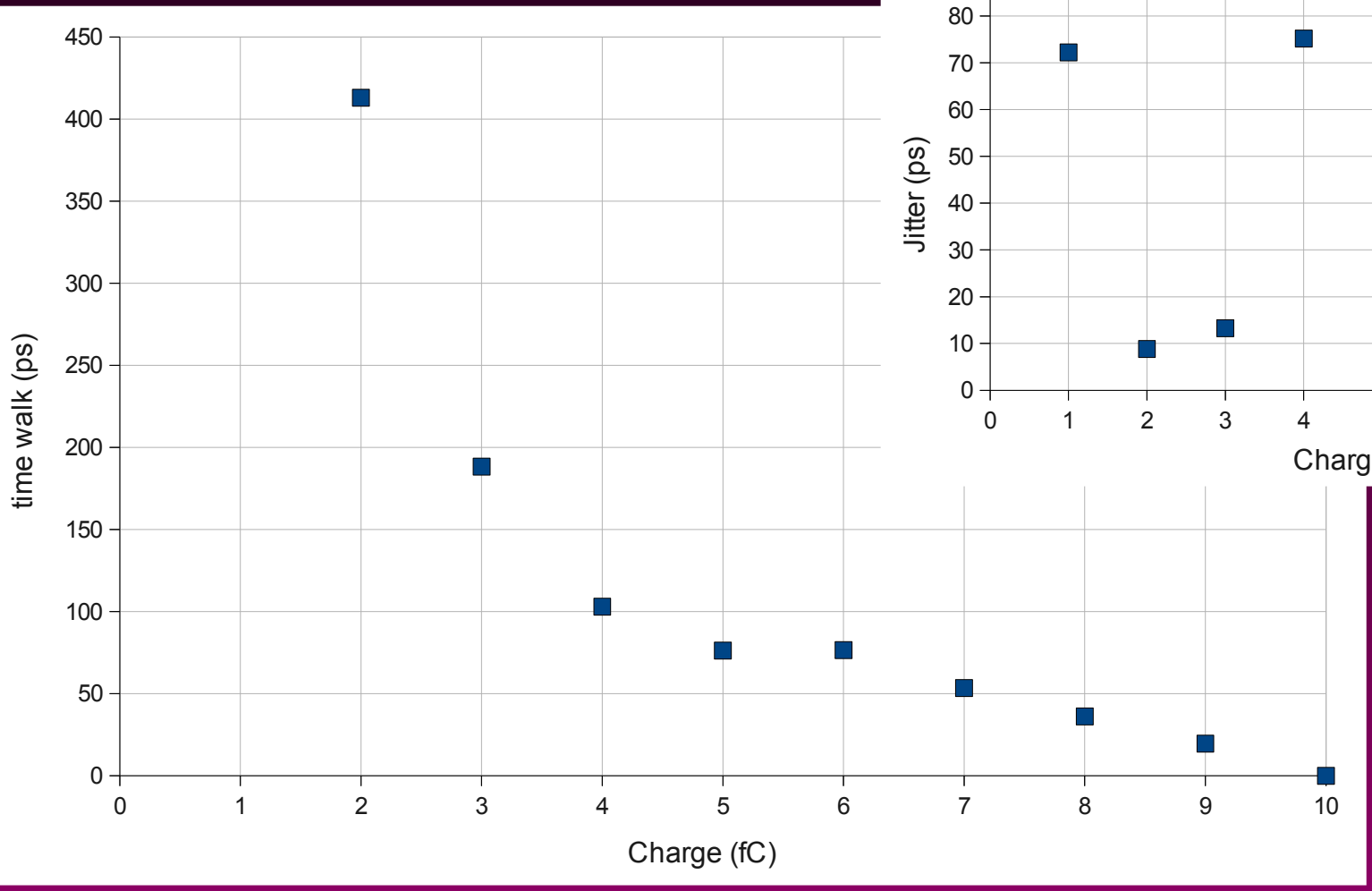

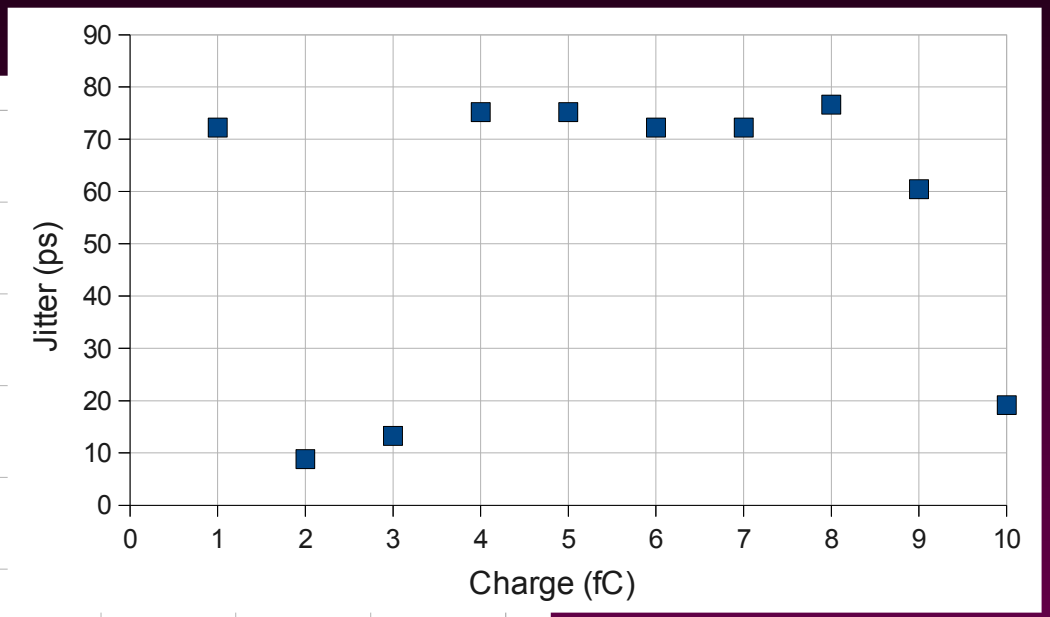

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Conclusions - 1

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Sezione di Torino

A 20 mm^2 prototype has been submitted. It includes :

- The 300 × 300 μm^2 full pixel cell with preamplifier, CFD, TAC, A/D conversion and control logic
- Two full size and one reduced size columns
- High speed clock distribution
- End of column buffering and flow control
- SEU protection

End of column multiplexing and high speed serializers are still missing

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Conclusions - 2

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Sezione di Torino

- Tests are ongoing – preliminary results look ok
- Three "hiccups" prevent us to have a rock solid proof of the complete chip functionality, however :
  1. the CFD alone provides sufficient time walk correction
  2. still in the specs for the TDC resolution
  3. accepting some data loss it is possible to work in Gray mode
  4. these hiccups will be easy to correct in the next version (no conceptual errors, just oversights)

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Activity - 2010

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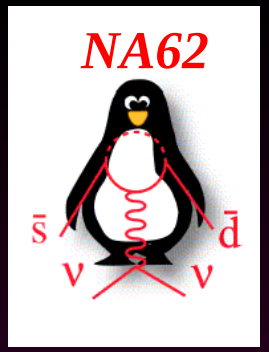
- Test pulse calibration and TDC linearity
- Gray decoding and tests
- FPGA based DAQ (Ferrara)
- Laser and beam test
- How to test high rate ?
  - beam test will not provide informations
  - HDL simulations



Activity - 2011

Sezione di Torino

Selected option : TAC based TDC

- chip responsibility & final verification → Torino
- 2nd prototype 1st half 2011
- support from CERN is of course welcome

Selected option : DLL based TDC

- chip responsibility & final verification → CERN
- interest in selected building blocks (e.g. serializer, calibration DACs)

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Spare slides

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Sezione di Torino

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Test features

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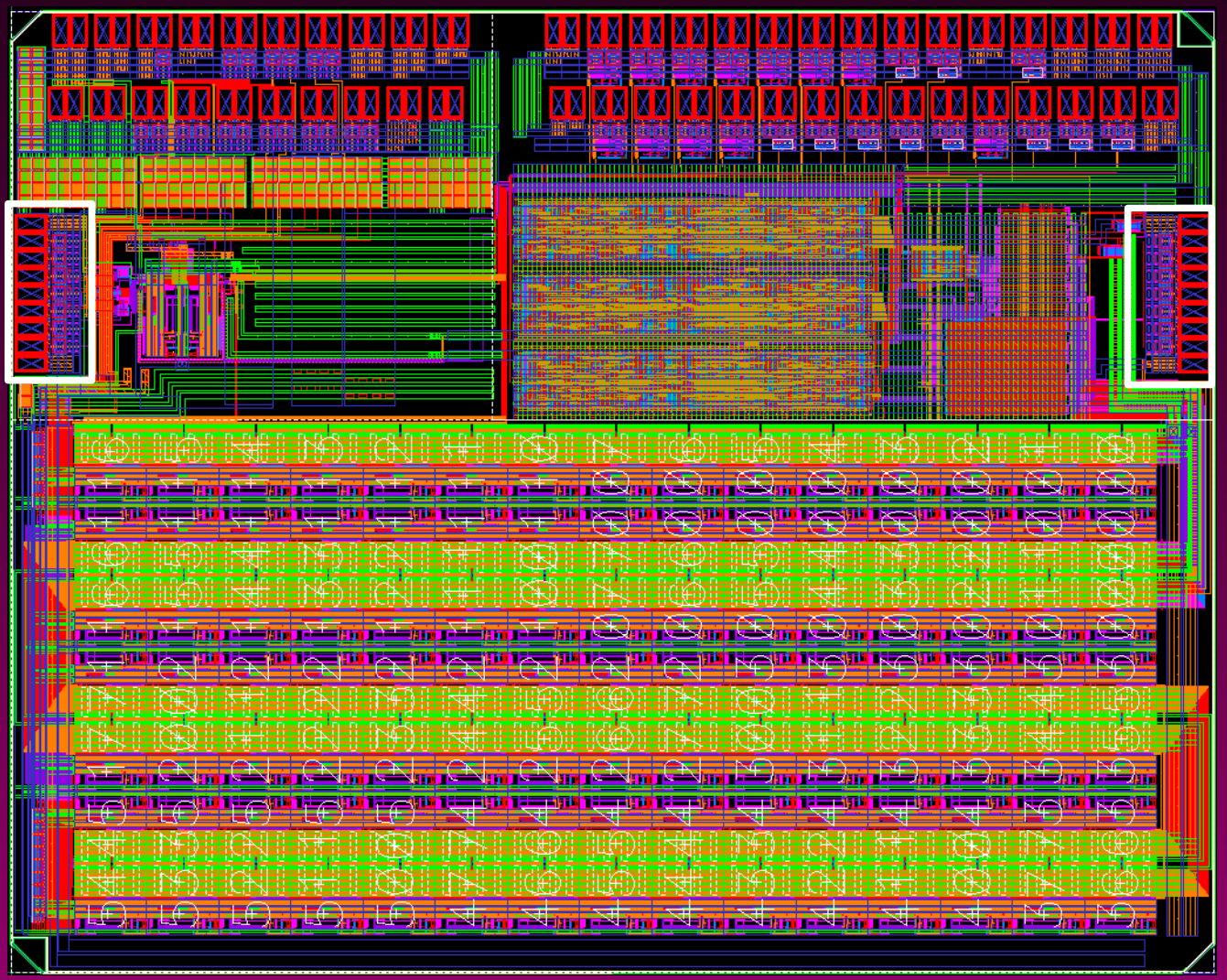
Analogue test pads



Digital test pads

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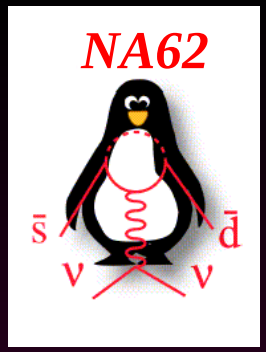

Analogue test features

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- The following signals of a spare analogue pixel cell are externally available via a multiplexer :
  - preamplifier output
  - CFD output
  - TDC output
- The multiplexer is externally controlled
- These output are not available when the detector is connected

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Digital test features

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- 7 CMOS outputs available for testing of the end of column controller
- Outputs are tri-state, controlled by CCR[10]
- Either the 7 LSBs of the coarse counter or the status word from the 3 columns can be selected via CCR[1:0]
- For each column 24 bits are available for debugging. CCR[8:7] controls the multiplexing