P-TDC: test results update

Test results

Test setup status :

- DP+LSA test setup ok
- DG2020 calibration ongoing
- FPGA-based DAQ under development (Ferrara)
- Beta version available

Test status :

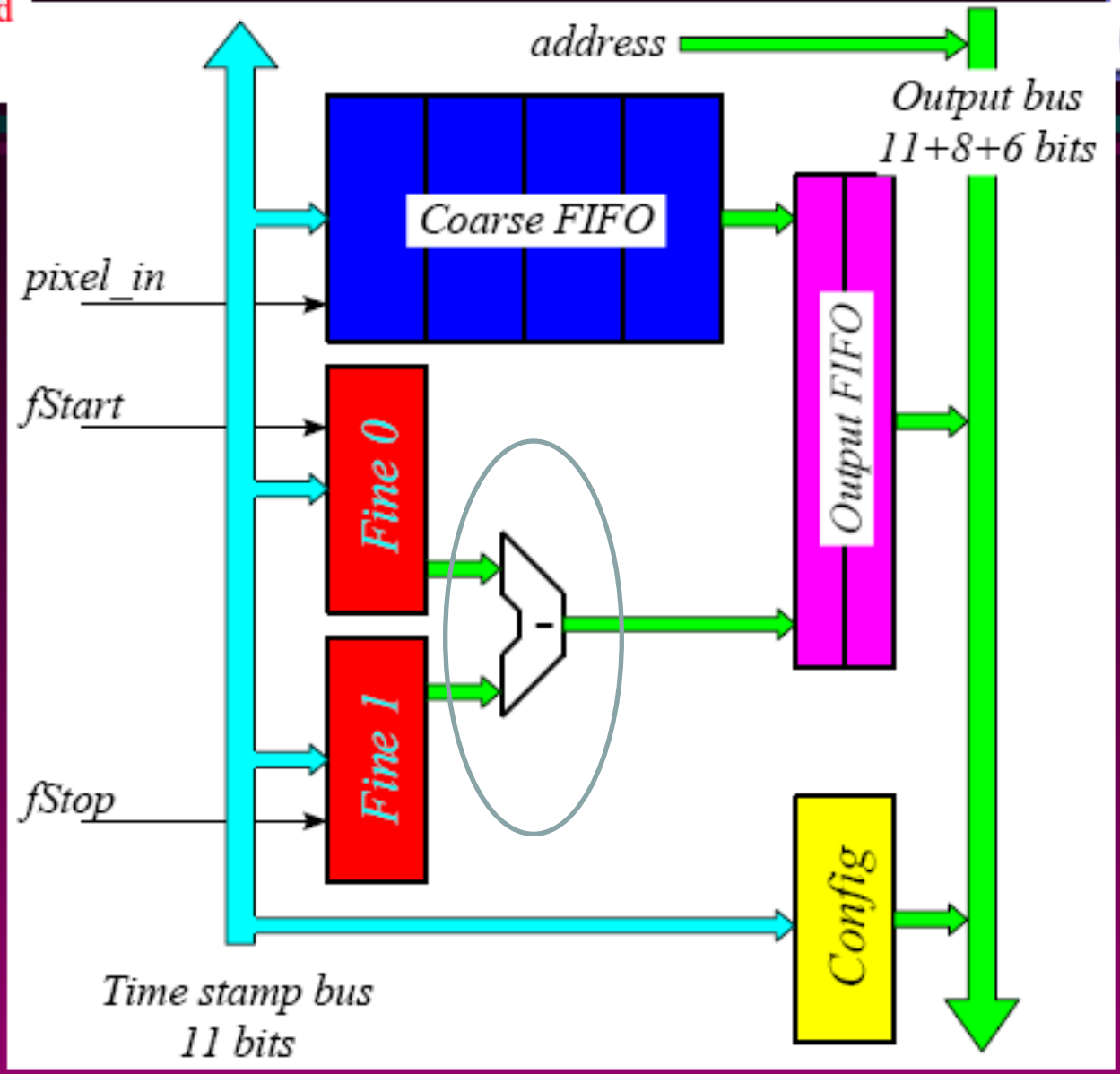
- Pixel equalization done
- Efficiency and jitter measurement done
- TDC linearity to be done

some new results

Hiccups...

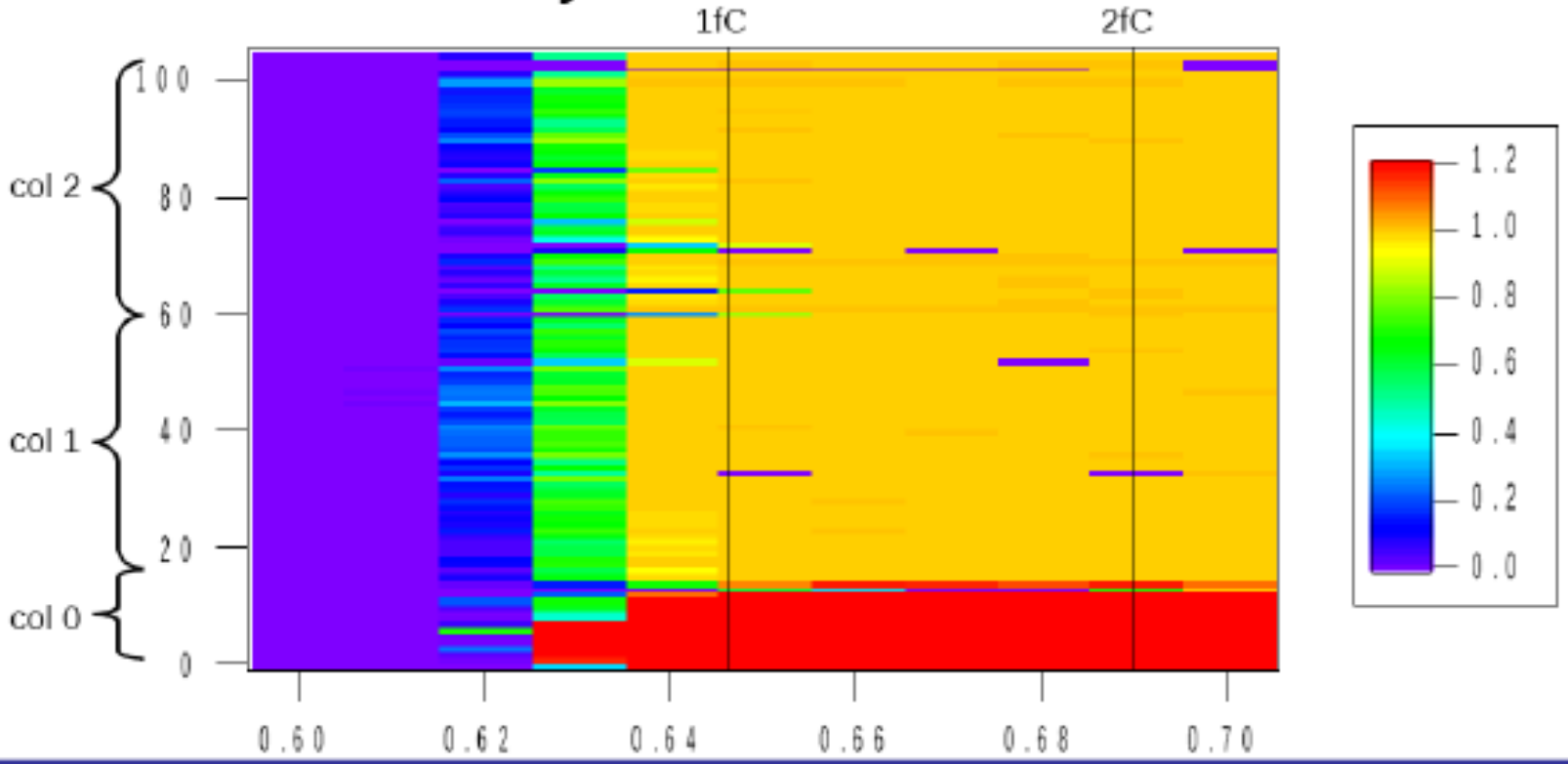
1. CFD output not correctly connected
   - Problem can be mitigated but not fully corrected.
   - CFD performances can be studied separately
2. Digital logic output driver undersized
   - Working frequency limited at 128 MHz @1.5 V
   - Time bin still in specs
3. Incorrect subtraction in Gray mode
   - Some data processing required to get the info
   - Some data to be discarded ?

Data conversion



Efficiency - 1

- Second equalization: full efficiency at 1fC, but column 0 noisy



Efficiency for a typical pixel as a function of the injected charge

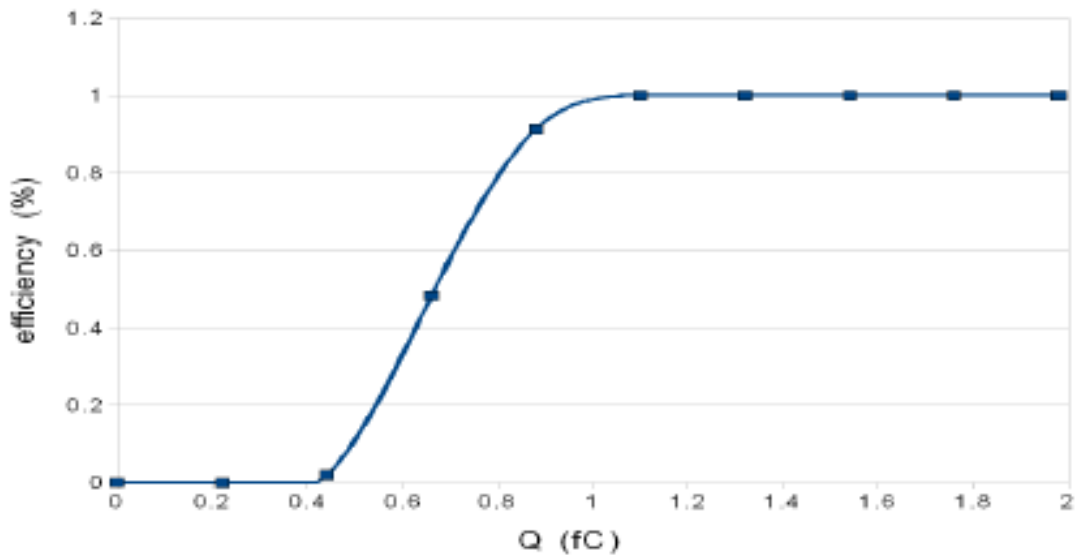


Figure 17: Efficiency curve for one pixel.

Jitter measured out of the full chain:

a) Charge injection with a fixed phase with respect to the clock
b) Measurement of the fine time
c) Consider the time distribution and compute the time resolution adding in quadrature bin-width/sqrt(12) = 40 ps

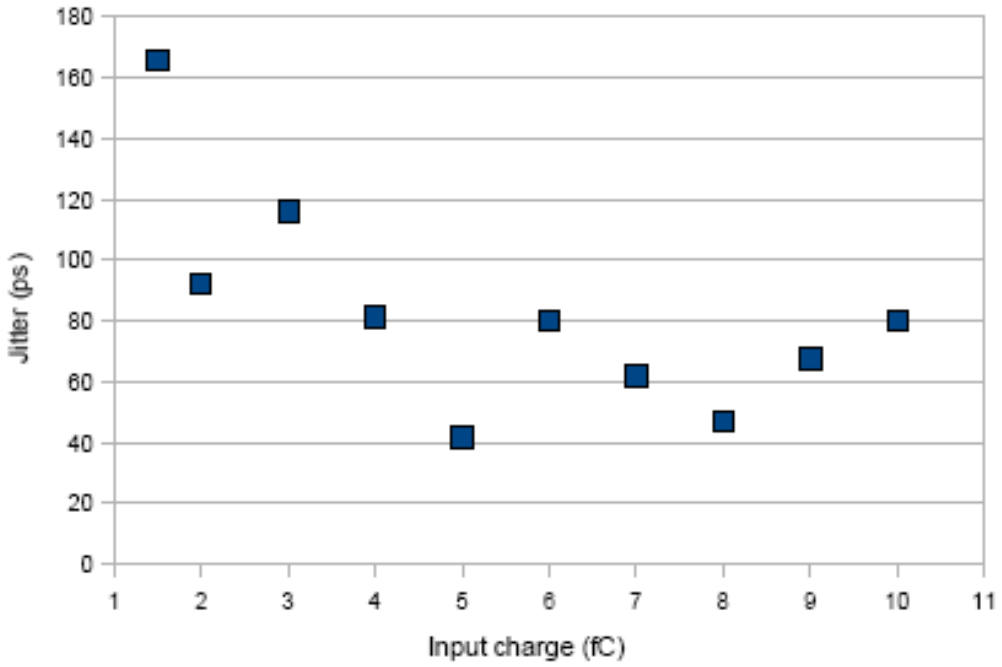


Figure 22 System jitter at 128 MHz clock.

TDC populated with a 10^5 pulses with random phase

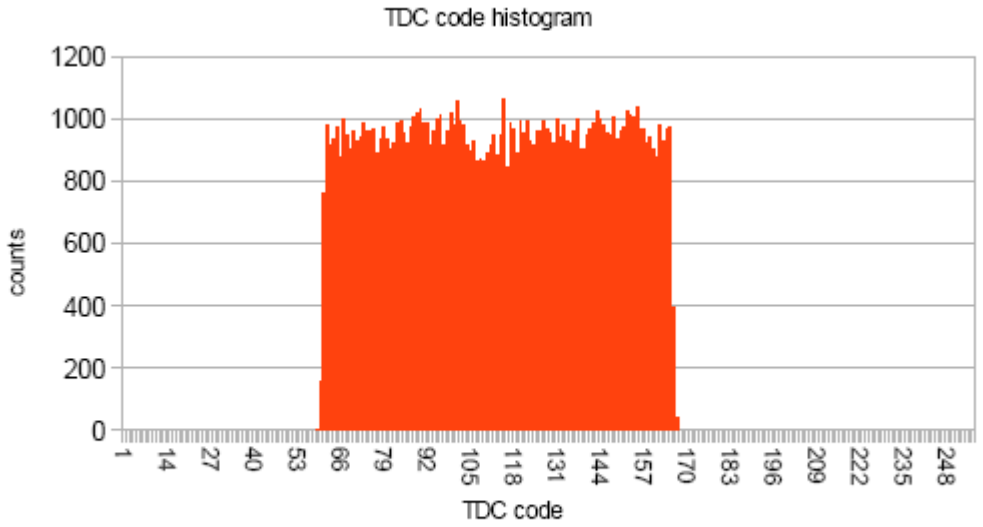


Figure 18: Example of raw code distribution used in the calculation of TDC DNL and INL from a data sample of 100.000 events.

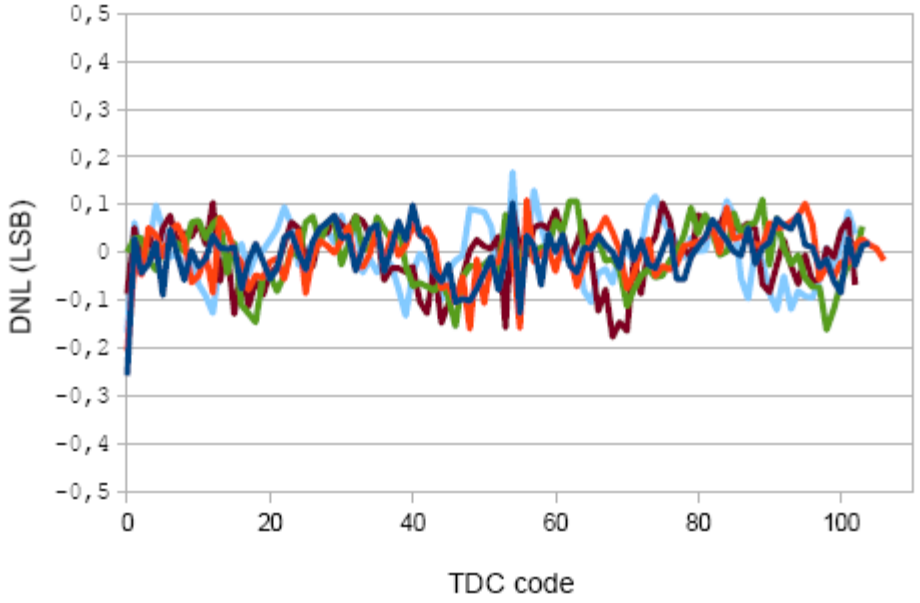


Figure 19: Differential non-linearity of five different TDCs from the matrix.

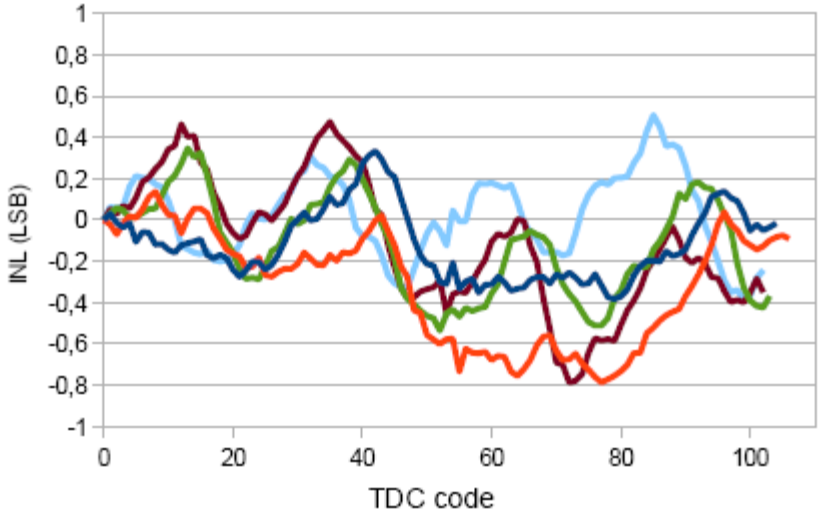


Figure 20: Integral non-linearity of five different TDCs from the matrix.

Residual time-walk of the CFD measured with the LSA

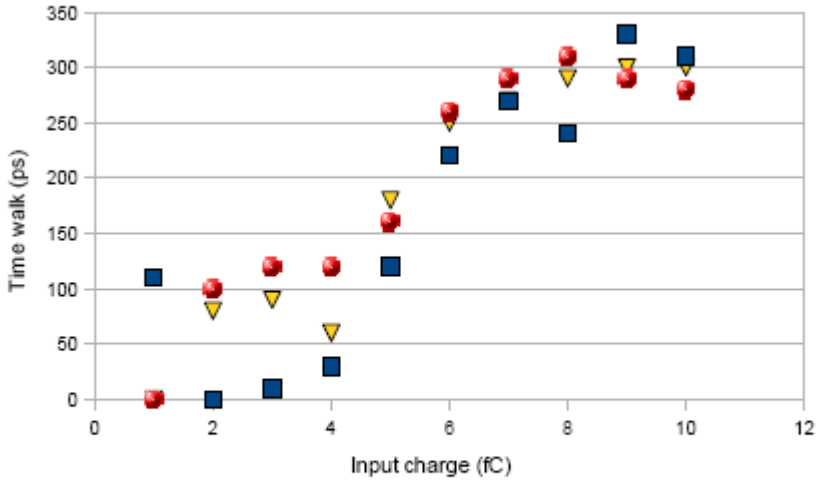


Figure 21 Residual CFD time walk at different clock frequencies

Figure 21 shows a measurement of the residual time walk of the CFD taken at different clock frequencies (blue squares=no clock, yellow triangles=160 MHz, red squares=320 MHz). Figure 22 shows the jitter measured in the range 1.5-10 fC. The measurement was done at the clock frequency of 128 MHz.

DAQ-prototype status

(from S. Chiozzi-Fe)
-FPGA firmware: ready
The new version has been delivered on Friday and has to be tested in Torino

-DAQ software for final system with 4-nodes: under development
Need to address the four FPGA cards

-Trigger system for GTK-DAQ-RUN-2010: to be done

Conclusion

1. The building blocks have been checked.
2. All behaves within specifications
3. So far no show stoppers
4. There are several hiccups that will make complete tests difficult and one has to analyze some blocks individually
5. Full characterization is underway

Technical Advisory Panel

Some experts on the field will be asked to scrutinize both options and give a recommendation or simply the pros and cons of both solutions.

Experts: Campbell, Horisberger, Musa, Snoeys
They are going to be contacted asap