A recently developed silicon wafer bonding technique has been proposed. This new process would enable direct bonding of a read-out electronic chip wafer on a highly resistive silicon substrate wafer. Therefore, monolithic silicon detectors could be fabricated in this way. This would allow the free choice of electronic chips and high resistive silicon bulk, even from different providers. Moreover, a monolithic detector with a massive high resistive bulk could be obtained. Electrical properties of the bonded interface are critical for this application. Indeed, mobile charges generated by radiation inside the bonded bulk are expected to transit through the interface in order to be collected by the read-out electronics. In order to characterize this interface, the concept of Transient Current Technique (TCT) has been explored by means of numerical simulations combined with a physics based analytical model. For this purpose, we have considered a simple PIN diode reversely biased where the high resistivity active region of interest is set in full depletion. First, Synopsys Sentaurus TCAD is used to determine if TCT such as it may be performed in bonded interfaces characterizations is well sounded. Next, the analytical model is used to give a better insight into the physics behind the TCT when interface layers with traps are introduced. This technique is expected to be relevant to characterize key parameters such as the charged traps concentration in of bonded interfaces.