**Belle-II Silicon Vertex Detector**

Presenter: Deepanwita Dutta, TIFR, Mumbai (on behalf of the Belle-II SVD group)

**Abstract:**

The Belle II experiment at the SuperKEKB collider in Japan will operate at an unprecedented luminosity of $8 \times 10^{35} \text{ cm}^2 \text{s}^{-1}$, about 40 times larger than its predecessor Belle experiment. Its vertex detector is composed of two-layer DEPFET pixel detector (PXD) and four-layer double-sided silicon microstrip detector (SVD). To achieve a precise decay vertex position determination and excellent low-momentum tracking, even under the high background and high trigger rate of 10 kHz, the SVD employs several innovative techniques. In order to minimize the parasitic capacitance in the signal path, 1,748 APV25 ASIC chips, which read out signals from 224k strip channels, are directly mounted on the modules with the novel Origami concept. The analog signals from APV25 are digitized by a flash ADC system, and sent to the central DAQ as well as to online tracking system based on SVD hits to provide the region of interests to PXD for reducing the latter’s data size to achieve the required bandwidth and data storage space. In this talk, we present the design principles and construction status of the Belle II SVD.