First production of Ultra-Fast Silicon Detectors at FBK

Segmented silicon sensors with internal gain, the so called Ultra-FAST Silicon Detectors (UFSD), have been produced at FBK for the first time. UFSD are based on the concept of Low-Gain Avalanche Detectors (LGAD), which are silicon detectors with an internal, low multiplication mechanism (gain ~ 10) so that they will provide the traditional silicon sensor benefits (segmentation, low leakage current, low noise, low capacitance) together with a much larger signal.

We have designed and manufactured on high resistivity, 275 µm thick 6” FZ silicon wafers a production of LGAD sensor using a fully double-sided technology. This production houses two main type of devices: one type where the gain layer is on the same side of the read-out electrodes, the other type where the gain layer is on the side opposite to the multiplication layer (reverse-LGAD). We have manufactured 12 wafers, with 5 different doses of the gain layer implant, to study the performances of the sensors with various levels of signal amplifications. The production required 12 photolithographic masks. All the doped regions have been obtained by means of ionic implantation: arsenic has been used for the formation of the shallow front n++ region, while Boron has been implanted in order to define the gain layer and the p++ segmented region.

Several detector geometries have been investigated in this first production, including single pad of various sizes, with active area from 0.25 to 25 mm², different pad array geometries, and large pad array and micro-strip structures, both LGAD and reverse-LGAD.

In this production we have also explored the possibility of obtaining position information via AC coupling: the resistivity of the ohmic p++/p contact has been tailored so that the signal is AC induced to the read-out pads. This design allows having a very uniform electric field, while keeping the possibility of fine electrode segmentation. The delicate aspect of this design is the capability of matching the p++ resistivity with the value of the coupling capacitance so that the signal will correctly be transferred to the electronics.

We have performed extended testing on the wafers and the results are in line with simulations: the two lower gain splits show good performances, with break-down voltages above 1000 V, while the higher density implants, generating more gain, show a lower break down voltage. Up to the second highest implant, a bias voltage in excess of 500 V was reached. All the tested devices show a very low excess noise factor.

Additional testing of beam test performances, AC coupled devices, reverse-LGAD and radiation hardness are currently being carried on, and will be available in the next months.