GBCR2 Status
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Oct 8th 2019
ATLAS ITK Pixel Electronics Meeting
Outline

• Feedback from PDR
• Equ in uplink channel
• Downlink channel design
• DC-offset cancellation design
• Pad/package update
• Plan/Summary
Feedback from PDR

1. Increasing the gain should reduce the impact of the stages offset and will also result in better noise performance.

2. Operating at 1.28 Gb/s should also allow to use simple CTLE stages instead of the LFEQ stage, reducing the power consumption and improving the noise. A unity gain setting, for the full chain, should also be envisaged.

3. DC coupling should not be needed if the gain of the equalizer stages is increased. In case this is not possible, please simulate the DC wander by using realistic 64B/66B frames.

4. Another alternative to control the DC offset, in case the gain can’t be increased, will be to use a feedback loop to control the DC offset build-up in the equalizer. Please note however that this also introduces a low frequency zero and thus has similar problems to the AC coupling.

5. To balance the power and ground pads having power - ground side by side instead of ground - ground and power-power. Placing additional GND pads between neighboring differential pairs (on input and output side) would improve crosstalk isolation.

All are good suggestions for design improvements.
Revision in design

• Equ channel: Remove LFEQ stage and use multiple stages of CTLE. We keep the DC gain of each stage around unit gain so that the Equ output amplitude does not attenuate too much.
• Add downlink for 160 Mbps signal
• Considering removing AC coupling with low-pass filter to cancel DC-offset.
• Update pads of the chip including Ground/Power pads.
The signal loss of 6-m cable plus 1m Flex

- We divide the signal loss curve in 3 ranges:
  - High Frequency range: 0.4-1.3 GHz, slope is **27.3 dB/decade**, need a multiple order CTLE (two or three orders)
  - Middle Frequency range: 0.2 to 0.4 GHz, slope is **14.3 dB/decade**, one order CTLE
  - Low Frequency range: 0.8 to 0.2 GHz, slope is **8.5 dB/decade**, one order CTLE
Refined Equ Design

- 3 stages of high frequency CTLE. Zero=540M, Pole1=1.5G
- 1 stage of medium frequency CTLE. Zero=170M, Pole1=450M
- 1 stage of low frequency CTLE. Zero=120M, Pole1=170M.
Equ Layout

Size: 143u * 66u
The DC gain degenerated about 5dB for longest cable (original design is about 20 dB).
The DC gain improvement slightly improves the mismatch.
EQ Simulation (10cm Flex + 3m Twinax)

Pre-layout Results
Config: 4’b0100
Jitter = 40 ps

Post-layout Results
Config: 4’b0100
Jitter = 22 ps
EQ Simulation (1m Flex + 6m Twinax)

Pre-layout Results
Config: 4’b1011
Jitter = 71 ps

Post-layout Results
Config: 4’b1011
Jitter = 60 ps
PVT Result (Post-layout, 1m Flex+6m Twinax)

- Typical & 27Degree & 1.2V Power
  Config: 4'b1011
  Jitter = 60 ps

- Slow & 100Degree & 1.08V Power
  Config: 4'b1111
  Jitter = 94 ps
• The AC coupler does not fully remove DC-offset. The new DC offset cancelation circuits is in progress.
Pattern Result (Post-layout, 1m Flex+6m Twinax)

Config: 4'b1011, typical corner

1. PRBS10, Jitter=60ps
2. PRBS31, Jitter=66ps
3. PRBS61, Jitter=66ps
DC-offset cancellation

• A RC filter is used to filter the high-frequency signal and a differential amplifier will sense the DC-offset and correct it in the feedback.

• We will take advantage of Miller effect to reduce the filtering capacitor size
• In the LPF filter, $R=1.5$ Mohm, $C = 4$ pF. The opamp gain is 60 dB.
• Due to the mismatch from feedback circuits can not be corrected, the layout has to be mismatch-aware. A common-centroid layout will be done.
The DC-offset cancellation circuit senses the DC-offset at the output of LA and feedback to the input of LA.
Open loop response

- The phase margin is 69 degree
• The low cut-off frequency is 115 kHz, good enough for 1.28 GHz and 160 MHz data transmission.
DC cancellation in transient simulation

Input eye, shift up positive signal 50 mV more than negative signal

Feedback signal converge slowly due to LPF
The feedback signal is not more than 7 mV.
The output eye is not converged in 40 us simulation. But it is on the right direction. We will see the final results soon.
Downlink Channel Design

- 2 stages of pre-emphasis and 1 stage of output driver.
- A DC-offset cancellation will be added to remove the duty-cycle distortion (DCD) jitter from mismatch circuits and input as well.
Schematic of Downlink channel

For the longest cable,

Rs1 = 1.5 KOhm  
Cs1 = 3 pF  
Zero = 35M, pole1 = 53M

Rs2 = 2.5 KOhm  
Cs2 = 1.5 pF  
Zero = 42M, pole = 110 M
Pre-emphasis AC response

Peaking strength:
2.5 dB ~ 14.8 dB @160M
AC Response of Downlink Channel with cable

Red line: 10cm Flex + 3m Twinax
Config: 3'b010

Green line: 1m Flex + 6m Twinax
Config: 3'b101
Downlink results (comparison with GBCR1)

Downlink channel in GBCR2
1m Flex + 6m Twinax
Jitter = 156 ps

Downlink channel in GBCR1
6m Twinax
Jitter = 345 ps
Eye diagram to RD53 after cables

Typical corner
1m Flex + 6m Twinax
Config: 3’b101
Jitter = 156 ps

Typical corner
10cm Flex + 3m Twinax
Config: 3’b010
Jitter = 88 ps
Downlink results (PVT)

Fast & n20 Degree & 1.32V Power
1m Flex + 6m Twinax
Config:3’b101
Jitter = 161 ps

Slow & 100Degree & 1.08V Power
1m Flex + 6m Twinax
Config:3’b101
Jitter = 240 ps
Pads update

• The die size increases to 1mmx3mm
• We add two downlink channels. Total 62 pads on the die.
Package update

- QFN-40 has not enough pins, we choose QFN-48 pin
- We add grounding pads between two adjacent channels
- We remove one test pin and keep 4 power supply pins
- We have confirmed that the bonding diagram works from manufacture in production process.

<table>
<thead>
<tr>
<th></th>
<th>Pads</th>
<th>Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX channels</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>RX channels</td>
<td>28</td>
<td>28</td>
</tr>
<tr>
<td>I2C</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Clock in</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Test</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Power</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Ground</td>
<td>14</td>
<td>0</td>
</tr>
<tr>
<td>Total</td>
<td>62</td>
<td>48</td>
</tr>
</tbody>
</table>
## GBCR2 jitter estimation

<table>
<thead>
<tr>
<th>Mode</th>
<th>Input Jitter from RD53 (ps)</th>
<th>Jitter from cable+GBCR (ps)</th>
<th>Estimated Output jitter to lpGBT (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx Equalizer mode</td>
<td>100</td>
<td>81</td>
<td>181</td>
</tr>
<tr>
<td>Rx Retiming mode</td>
<td>11</td>
<td>11</td>
<td>80</td>
</tr>
</tbody>
</table>

- The input jitter from RD53 is dominated by its recovered clock (<100 ps).
- The retiming clock signal is from lpGBT and its jitter is 5 ps (RMS).
- In the retiming mode, the output jitter is $11 + 5 \times 14 = 80$ ps
## Power Consumption update

<table>
<thead>
<tr>
<th></th>
<th>Equalizer mode (mA)</th>
<th>Retiming mode (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equalizer</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>LA</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>CML driver ( @ 200mV)</td>
<td>4.0</td>
<td></td>
</tr>
<tr>
<td>Downlink</td>
<td>15.3</td>
<td></td>
</tr>
<tr>
<td>Retiming DFF</td>
<td>0</td>
<td>1.0</td>
</tr>
<tr>
<td>I2C</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>phaseshifter</td>
<td>0</td>
<td>15.3</td>
</tr>
<tr>
<td>Full chip (6 Rx+2 Tx)</td>
<td>65.8</td>
<td>87.1</td>
</tr>
</tbody>
</table>
# GBCR2 specification

<table>
<thead>
<tr>
<th></th>
<th>Uplink</th>
<th>Downlink</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data rate</strong></td>
<td>1.28 Gbps,</td>
<td>160 Mbps</td>
</tr>
<tr>
<td><strong>Channels</strong></td>
<td>Up to 7</td>
<td>Up to 2</td>
</tr>
<tr>
<td><strong>Low cut-off frequency</strong></td>
<td>&lt; 200 kHz</td>
<td></td>
</tr>
<tr>
<td><strong>Input impedance</strong></td>
<td>50 ohm (typical)</td>
<td></td>
</tr>
<tr>
<td><strong>Output impedance</strong></td>
<td>50 ohm (typical)</td>
<td></td>
</tr>
<tr>
<td><strong>Input signal amplitude</strong></td>
<td>&gt;400 mV in differential (note 1)</td>
<td>&gt;400 mV in differential</td>
</tr>
<tr>
<td><strong>Input signal jitter</strong></td>
<td>&lt; 100 ps (note 1)</td>
<td>Expected to remove input DCD jitter</td>
</tr>
<tr>
<td><strong>Output signal amplitude</strong></td>
<td>200 mV in differential</td>
<td>200 mV in differential (typical) (note 2)</td>
</tr>
<tr>
<td><strong>Output signal jitter</strong></td>
<td>&lt; 100 ps (pk-pk) in retiming mode ; &lt; 200 ps (pk-pk) in equalizer mode</td>
<td>&lt;250 ps (pk-pk)</td>
</tr>
<tr>
<td><strong>Flex Cable length</strong></td>
<td>0.1 to 0.5 meter</td>
<td></td>
</tr>
<tr>
<td><strong>TWINAX cable length</strong></td>
<td>3 to 6 meters</td>
<td></td>
</tr>
<tr>
<td><strong>Power consumption (typical)</strong></td>
<td>80 mW in equalizer mode (6 ch) ; 105 mW in retiming mode (6 ch)</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** For the input signal of Rx, measured jitter/amplitude without FLEX/TWINAX cable on scope.

**Note 2:** For the output signal of Tx, measured jitter/amplitude after FLEX/TWINAX cable on scope.
Summary/Plan

• Updated and improve Equ design
• Add two downlink channel design
• Updated Pads of GBCR2
• DC-offset cancellation circuits schematic is done, layout is ongoing
• Will submit design in Oct 23rd.