### Optoboard Modularity

<table>
<thead>
<tr>
<th>Optoboard ID</th>
<th>OBD-4</th>
<th>OBD-3</th>
<th>OBD-2</th>
<th>OBD-1</th>
<th>OBD-0</th>
<th>OBD-7</th>
<th>HCCDC</th>
<th>Cross-section ITK [cm²]</th>
<th>Defined connectivity between PP0’s and Optoboards/boxes</th>
<th>Whole Optoboxes can still be reallocated</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN-ITE-0</td>
<td>136</td>
<td>4094</td>
<td>915</td>
<td></td>
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<td>4</td>
<td>24</td>
<td>144 12</td>
<td>L1 Flat Barrel</td>
<td>L1 Flat Barrel</td>
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<td>144 12</td>
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<td>L1 End Cap</td>
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<td>915</td>
<td></td>
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<td>4</td>
<td>24</td>
<td>144 12</td>
<td>L2 Flat Barrel</td>
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<td>4094</td>
<td>915</td>
<td></td>
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<td>24</td>
<td>144 12</td>
<td>L2 Barrel Rings</td>
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<td>L3 Flat Barrel</td>
<td>L3 Flat Barrel</td>
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<tr>
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<td>4094</td>
<td>915</td>
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<td>4</td>
<td>24</td>
<td>144 12</td>
<td>L3 Barrel Rings</td>
<td>L3 Barrel Rings</td>
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<td>AN-ITE-7</td>
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<td>4094</td>
<td>915</td>
<td></td>
<td></td>
<td>4</td>
<td>24</td>
<td>144 12</td>
<td>L4 Flat Barrel</td>
<td>L4 Flat Barrel</td>
</tr>
</tbody>
</table>

### Optoboard System Status

- **OBD-1 to OBD-7**
- **HCCDC total DCDC12V**: 136
- **total lpGBT**: 4094
- **total uplinks**: 915
- **Cross-section ITK [cm²]**: 55.17582
- **Cross-section L4 [cm²]**: 55.17582

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**Work by Antonello and me**

5. June 2019

Armin Fehr (LHEP)
Prototypes
Heat dummies to simulate heat dissipation in Optobox
→ Test feasibility of cooling and cabling strategy
Read out component temperatures and humidity via Arduino
Optoboard V0

- 1 VTRx+, 1 LpGBT, 1 FEAST 1.2V DCDC
- Delays due to difficulty of finding capable vendor
- Now submitted to HiTech (Macedonia), expect 30 boards end-June
Powerboard V0

- Powering of Optobox V0 through FEAST 10V to 2.5V converters
- Submitted, arriving mid-June
- Replace FEAST by bPol12V for Powerboard V1
Component tests
VTRx+ Test Setup

- Bit error rate test of VTRx+
- I2C control of VTRx+
- Communication to FPGA board over USB Uart
VTRx+ Characterisation Results

BER test at 10 Gb/s, default settings (Pixel Electronics Meeting 27.02.2019)

Optical eye at 10 Gb/s, default settings (Pixel Electronics Meeting 3.4.2019)

→ VTRx+ performance within specifications

Qualification task item
Adapting LpGBT-fpga backend firmware into VTRx+ test setup

Using LpGBT emulator until Optoboard V0 arrives

Communication chain LpGBT-fpga – Optoboard V0 – LpGBT-fpga

Qualification task item
LpGBT Tests (2/2)

- LpGBT-fpga generates downlink data, sent over SFP+ – VTRx+ – FMC
- LpGBT emulator receives downlink data, locks to header, generates uplink data, sends back over FMC – VTRx+ – SFP+
- LpGBT-fpga receives uplink data
- Now working on register r/w of LpGBT via IC-field of downlink
Integrate RD53A emulator into Optoboard test setup

Send sync pattern and trigger over downlink, receive generated data

Work done by Bachelor Student Dominique Roux
FMC Adapter for elinks

- ERF8 (Optoboard elink connector) to FMC Adapter
- Access to elinks and LpGBT control and status signals from KC705
- Submitted, will arrive end-June

Qualification task item
Work starting up, I2C configuration currently

Goal:
- Interface to Optoboard V0 and RD53A emulator via SMA
- Test functionality of readout chain and BER test with twinax/flex cable
- Power GBCR with FEAST DCDC

PhD Student Meghranjana Chatterjee working on it
Getting experience with DCDC converter similar to bPol modules (not yet available)

FEAST DCDC converter at $V_{out} = 2.5\,\text{V}$

- FEAST performance within specifications, load regulation better for bPol DCDC

Work done by Master Student Roman Müller
Twinax Cable Test

<table>
<thead>
<tr>
<th>$S_{ddz1}$ [dB]</th>
<th>Initial</th>
<th>1 cycle</th>
<th>3 cycles</th>
<th>10 cycles</th>
<th>SLAC</th>
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<tbody>
<tr>
<td>640 MHz</td>
<td>-10.6 dB</td>
<td>-10.6</td>
<td>-10.6</td>
<td>-10.6</td>
<td>-10.9</td>
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<tr>
<td>2.5 GHz</td>
<td>-21.7 dB</td>
<td>-21.6</td>
<td>-21.7</td>
<td>-21.7</td>
<td>-22.1</td>
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<tr>
<td>3.2 GHz</td>
<td>-24.7 dB</td>
<td>-24.7</td>
<td>-24.8</td>
<td>-24.8</td>
<td>N/A</td>
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<tr>
<td>5 GHz</td>
<td>-31.5 dB</td>
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<td>-31.7</td>
<td>-31.7</td>
<td>-32.5</td>
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</tbody>
</table>

- Bending test and S-parameters after 1, 3 and 10 thermal cycles (−70 °C to 20 °C)
- No visible damage after bending tests
- Irradiation to 10 Mrad mid-June
- Irradiation to 300 Mrad until end of June
- Thermal cycles and S-parameter test after irradiation

Work done by Akitaka Ariga
Summary

- Optical fan-out ✓
- Optoboard V0 ✓
  - VTRx+ ✓
  - LpGBT ✓
  - GBCR ✓
  - bPol12V and bPol2V5 ✓, comparable FEAST DCDC ✓
- Optobox V0 ✓
  - Thermal tests and cooling tests ✓
  - Updated cabling strategy ✓
- Power board V0 ✓
- Twinax cable ✓
- RD53 ASIC ✓, but RD53A emulator ✓

✓: Component not yet available
✓: Testing starts
✓: Testing done
Outlook

- **Optoboard V0 (VTRx+, 1 LpGBT, FEAST) tests this summer**
- **Build up communication chain LpGBT-fpga – Optoboard V0 – GBCR – Twinax – Flex – RD53 → until PDR (October 25th)**
- **Designs for PDR**
  - Optoboard V1 (VTRx+, 4 LpGBT, 4 GBCR, bPol2V5)
  - Power board V1 (bPol12V)
  - Optobox V1
Thank you!
Schematics of I2C control and BER test of the VTRx+

KC705 Evaluation Board

- FPGA
  - I2C Controller
  - IBERT IP Block
  - GTX Transceivers
- USB to Uart Bridge
- USB Jtag for FPGA config
- Computer
  - USB Uart

Carrier Board

- FMC
  - LDQ10 x4
  - VCSEL x4
  - GBTIA
  - PIN Diode
- SFP+
- Variable Optical attenuator
- Uplink: 
  - Fiber x1
- Downlink: 
  - Fiber x4
  - TX
  - Ethernet
### Comparison with VTRx+ specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Our measurement</th>
<th>VTRx+ Specs</th>
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<tbody>
<tr>
<td>OMA [dBm]</td>
<td>1.23</td>
<td>&gt; -5.2</td>
</tr>
<tr>
<td>Extinction Ratio [dB]</td>
<td>∼ 8</td>
<td>&gt; 3</td>
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<tr>
<td>Eye opening [%]</td>
<td>79</td>
<td>&gt; 60</td>
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<tr>
<td>Rise time [ps]</td>
<td>32.3</td>
<td>&lt; 44</td>
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<tr>
<td>Fall time [ps]</td>
<td>46.7*</td>
<td>&lt; 44</td>
</tr>
<tr>
<td>TJ (1e-12) [ps]</td>
<td>51.1</td>
<td>&lt; 25</td>
</tr>
<tr>
<td>DJδδ [ps]</td>
<td>40.81</td>
<td>&lt; 12</td>
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</table>

### High-speed signal path
- GTX transceivers driving PRBS signal
- High-speed lines on carrier board V0 hosting VTRx+
- Optical-electrical converter

* Not corrected for overshoot
# VTRx+ specifications

<table>
<thead>
<tr>
<th>#</th>
<th>Specification</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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<td>4.1.1</td>
<td>Tx OMA</td>
<td>-5.2</td>
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<td>dBm</td>
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<td>%(^a)</td>
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<td>850</td>
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<td>100</td>
<td>110</td>
<td>(\Omega)</td>
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<td>Rx Sensitivity(^c)</td>
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