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CMS Muon Endcap Track Finder DAQ readout format

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2015-12-03

The format is designed to easily interface with a 64-bit readout system through AMC13 card. This requires that all data sent to the AMC13 be an integer multiple of 64-bit words.

The Event Record has the following structure:

Table 1: Event record structure

Name	Size, 64-bit words
Event Record Header	3
Block of Counters	1
ME Track segments data	Variable, depends on presence of valid track segments and number of time bins requested
RPC primitives data	Variable, depends on presence of valid RPC primitives and number of time bins requested
SP track output data	Variable, depends on presence of detected tracks and number of time bins requested
Event record trailer	2

Table below lists maximum SP Event Record sizes in 64-bit words for 0 to 7 Time Bins.

Table 2: Maximum SP Event Record sizes for 0 to 7 TBIN values

TBIN	64-bit Words
0	6
1	126
2	246
3	366
4	486
5	606
6	726
7	846

Maximum Event Record size is 6 64-bit words for Headers/Counters/Trailers plus 120 64-bit words per a TBIN. For TBIN=7, event size comes to 846 64-bit words in total. At 10 Gbps DAQ line rate, the maximum size DAQ block will take 7.05 uS to transmit. Note that vast majority of the DAQ blocks will be much smaller (order of magnitude or more) because for a typical event just a small fraction of track segments is valid.

The main DAQ path in the upgraded Trigger system is AMC13 board. These boards receive information in 64-bit words. The tables in this document are organized in 16-bit notation. Each table contains a multiple of 4 16-bit words. The output 64-bit words are composed from 16-bit words as shown below:

Table 3: 64-bit word representation

Bits	[63:48]	[47:32]	[31:16]	[15:0]
16-bit word index	d	c	b	a

Bit 15 of each 16-bit word is used as section identifier. In each resulting 64-bit DAQ word, these bits (numbers 63, 47, 31, 15) form a unique ID code that should be used to identify the section type.

1. AMC data header

Each AMC in uTCA chassis must provide a header and a trailer according to this document, to satisfy AMC13 receiver:
http://ohm.bu.edu/~hazen/CMS/AMC13/UpdatedDAQPath_2014-07-10.pdf
MTF7 will form the AMC13 header and trailer as required.

2. Event Record Header

The Event Record Header consists of 3 64-bit words, where the most significant hex digit in each 16-bit word is the legacy DDU Code word 0x9 and 0xA. Green cells in Table 2 carry the SP-specific configuration settings; tan cells carry the SP-specific status; the content of all other cells complies with the legacy DDU requirement.

Table 4: Event Record Header

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0x9				L1A [11:0]												HD1a
0x9				L1A [23:12]												HD1b
0x9				0												HD1c
0x9				L1A BXN [11:0]												HD1d
0xA				0												HD2a
0xA				SP_TS[3:0]				SP_ERSV[2:0]			SP_ADDR[4:0]					HD2b
0xA				0	TBIN[2:0]			ddm	spa	rpca	skip	rdy	bsy	osy	wof	HD2c
0xA				ME1a[12:1]												HD2d
1							ME1b[9:1]									HD3a
0				ME2[11:1]												HD3b
0				ME3[11:1]												HD3c
0				ME4[11:1]												HD3d

Here:

- L1A [23:0] – Event Number picked from a 24-bit Event Counter;
- L1A_BXN [11:0] – Event Bunch Crossing Number (L1A arrival time) picked from a 12-bit Bunch Counter, running at TTC timing;
- SP_TS [3:0] – SP Trigger Sector 1, 2, 3, 4, 5, 6 for +Z EMU side and 7, 8, 9, 10, 11, 12 for –Z EMU side:

- SP_ERSV [2:0] = 0,…,7 – SP Event Record Structure Version;
    - SP_ERSV = 0 => initial draft 2014-07-15;
- SP_PADR [4:0] = 0..5 – SP Slot Number in uTCA chassis;
- DDM = 0 (default) / 1 – AMC13 (default) / PCIe Readout Mode.
- DD/CSR_DFC [10:0] = DAQ FIFO Configuration register:
    - RPCA = 0 / 1 (default) – RPC Active. If the bit is set to 1, then the RPC interface is considered to be ACTIVE;
    - SPA = 0 / 1 (default) – Sector Processor Active. If the bit is set to 1, then the Sector Processor output is considered to be ACTIVE and the DAQ block contains SP muon Track(s) SP1, SP2, SP3;
    - TBIN [2:0] = 0…7 (default = 4) – data collected from 0…7 Time Bins (bunch crossings).
- RDY, BSY, OSY, WOF – FMM signals Ready, Busy, Out-of-SYnch, Warning OverFlow.
- SKIP – if the SKIP bit is set to 1, then the Event Data is skipped for the current event, and the event shrinks to the Event Record Header, Block of Counters and Event Record Trailer only, as if the TBIN equals 0 (although actually not), see details on the L1A Finite State Machine (FSM) below.

- ME* are enable flags for all Muon Endcap CSCs. The notation is shown below:
    - ME means Muon Endcap
    - 1a, 1b, 2, 3, 4 is station number
    - index at the end is the CSC ID.
- RPC* are enable flags for RPC links. The notation is shown below:
    - RPC means Resistive Plate Chambers
    - Index at the end is link number

All FMM signals carry signal values at the time the current Event Record Header is composed, and NOT at the time L1A has been received. These signals are sent to FMM output.

3. Block of Counters

The Block of Counters consists of 2 30-bit counters:

- Track Counter;
- Orbit Counter.

Table 5: Block of Counters

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0	TC [14:0]															BCa
1	TC [29:15]															BCb
0	OC [14:0]															BCc
0	OC [29:15]															BCd

The Track Counter (TC) counts tracks found by the SP core logic and sent to the Muon Sorter (MS). It increments by 1, if only one track found; by 2, if 2 tracks found and by 3, if 3 tracks found in the current Bunch Crossing. The Orbit Counter counts LHC orbits to give time reference to the TC counter. Both counters are reset on an Orbit Counter Reset (OC0) TTC command. The counters are read out on L1A signal prior to be incremented by number of Tracks found or BC0 TTC command, either or both of

which may happen to be in the same Bunch Crossing.

4. Event Data

The Event Data consists of TBIN Data Blocks, if non-Zero Suppression mode is selected (SZ = 0):

The Event Data consists of 0 to TBIN Data Blocks with valid data, if Zero Suppression mode is selected (SZ = 1):

4.1 Data Block

The Data Block content is determined by the Event Configuration Word (DD/CSR _DFC) and the proper data and consists of the following:

- 1 64-bit ME Data word per each CSC EMU MEx LCT;
- 1 64-bit RPC Data word per each RPC partition
- 2 64-bit SP Data words per SPz Track;

Here:

- MEx is one of the following muon LCTs:
  - ME1a[9:1], ME1b[9:1], ME2[9:1], ME3[9:1], ME4[9:1]
  - **Muon order always goes from ME1a to ME4, indexes from 1 to 9.**

- RPCx denotes the data from RPC links [24:1]
  - **RPC order is from index 1 to 24**

- SPz is one of the 3 output Tracks:
  - SP1, SP2, SP3 => set (SPA = 1) to make Active for readout.
  - **Track order always goes from SP1 to SP3.**

4.1.1 ME Data Record

Each track segment is reported using one 64-bit word. Note that only valid segments are included into DAQ stream; invalid segments are skipped.

Table 6: MEx Data Record

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
1	Key wire group [6:0]							Quality [3:0]				CLCT pattern [3:0]				MEa
1	BC0	BXE	L/R	CSC ID [3:0]				CLCT key half-strip [7:0]								MEb
0	AFFF	CIK	NIT	ME BXN [11:0]												MEc
0	AFEF	SE	SM	EPC [3:0]				AF	Station [2:0]			VP	TBIN Num [2:0]			MEd

Here:

- CLCT Pattern # [3:0] – 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Quality [3:0] – LCT Quality;
- Key Wire Group [6:0] – 7-bit value indicates the position of the pattern within the chamber and runs from 0 to 111;
- CLCT Key half-strip [7:0] – 8-bit value is between 0 and 159;
- CSC ID [3:0] – 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- Station: ME station number. 0 = ME1a, 1 = ME1b, 2 = ME2, 3 = ME3, 4 = ME4;
- L/R – Left/Right bend bit indicates whether the track is heading towards lower or

higher strip number;

- BC0 – Bunch Crossing Zero flag marks that next BXN = 0;
- ME_BXN [11:0] – LCT Bunch Crossing Number (LCT arrival time) picked from a local 12-bit Bunch Counter and running at link timing;
    - AFFF – Alignment FIFO Full Flag, should be 0, if AF has been initialized successfully by RSYNC;
    - AFEF – Alignment FIFO Empty Flag, should be 0, if AF has been initialized successfully by RSYNC;
    - EPC [3:0] – the Error Propagation counter at the Alignment FIFO output accumulates the "Receive Error Propagation" occurrences since last RSYNC.
- VP – Valid Pattern bit;
- SE – Synch Error bit, as received;
- SM – Modified Synch Error bit; modification based on the Optical Link status, Alignment FIFO status and Bunch Crossing Counter status;
- AF – Alignment FIFO status bit. AF bit is reset to 0 on RSYNC or Soft Reset and is set to 1 if the Alignment FIFO fails to deliver a data frame on read request any time after that. This is a fatal persistent link error, since the link becomes no longer locked to the received data stream => the link goes "out of synch";
- BXE – LCT timing mismatch bit. It is set to 1 if LCT BXN0 (least significant bit of received LCT Bunch Crossing Number) does not match ME_BXN0 (least significant bit of the local Bunch Crossing Counter running at link timing and controlled by link BC0 timing mark) and is 0 otherwise. Note, the test is done for bunch crossings with valid LCTs only (VP is set to 1);
- TBIN Num [2:0] – data block Time Bin Number.
- CIK – Character is K flag from the serial link.
- NIT – Not In Table flag from the serial link.

4.1.2 RPC Data Record

Each RPC primitive is reported using one 64-bit word. Note that only valid primitives are included into DAQ stream; invalid segments are skipped.

Table 7: RPC Data Record

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0	Prt. Delay[2:0]			Partition Num [3:0]				Partition data [7:0]								RPCa
0	BCN [5:0]							EOD	LB [1:0]		Link Number [4:0]					RPCb
1	BC0			RPC BXN [11:0]												RPCc
0													TBIN Num [2:0]			RPCd

Here:

- Partition Data – description not available
- Partition Num – description not available
- Partition Delay – how many BX a given frame was delayed with respect to the BX from which the "partition data" originates.
- Link number – number of the optical link that this primitive was received on
- LB – description not available
- EOD - indicates that the data being sent is not complete.

- TBIN Num – data block time bin number

4.1.3 SP Output Data Record

Each output track is reported using two 64-bit words. Note that only valid tracks are included into DAQ stream; invalid tracks are skipped.

Table 8: SPz Output Data Record

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
1	HL	C	VC	Phi_full [11:0]												SP1a
0	VT	SE	BC0	0	0	0	0	Phi_GMT[7:0]								SP1b
1	BX [1:0]		Quality [3:0]				Eta_GMT [8:0]									SP1c
0	ME1_ID[5:0]						Pt [8:0]									SP1d
0	ME4_ID[4:0]					ME3_ID[4:0]					ME2_ID[4:0]					SP2a
1	TBIN Num[2:0]			ME4_TBIN[2:0]			ME3_TBIN[2:0]			ME2_TBIN[2:0]			ME1_TBIN[2:0]			SP2b
1	PT_LUT_address [14:0]															SP2c
0	PT_LUT_address [29:15]															SP2d

Here:

- Phi_full is the track's phi coordinate as measured on the innermost available station, full precision
- Phi_GMT is the track's phi coordinate as reported to GMT
- Eta_GMT is the track's eta coordinate as reported to GMT
- Pt is the track's transverse momentum (output of PT LUT)
- Quality is the track's quality code. Bit assignment is shown below:
  bit 0 = ME4 hits present
  bit 1 = ME3 hits present
  bit 2 = ME2 hits present
  bit 3 = ME1 hits present
- PT_LUT_address is the address of the PT LUT memory that was formed by track-finder logic
- HL if set to 1 indicates that the track is created by beam halo muon
- C is the track's charge
- VC if set to 1 indicates that the charge is valid
- BX are three least significant bits of BX assigned to this track
- MEx_ID fields show which track stubs (from corresponding MEx stations) were used to build this track. Value of 0 in these fields means that the track stub from that station was not used. Format of these fields is shown below:

ME1_ID format:

D5	D4..D1	D0
0 = Subsector 1 1 = Subsector 2	CSC ID	Track stub number

ME2,3,4_ID format:

D4..D1	D0
CSC ID	Track stub number

- ME1_TBIN, ME2_TBIN, ME3_TBIN, ME4_TBIN are delays applied to the track stubs to build this track.
- SE – Synchronization Error bit is an OR (or some other Boolean function => to be determined) of Modified Synch Error bits for 15 MEx LCTs and similar bits

for 2 MBy Stubs;

- BXN0 – an OR (or some other Boolean function => to be determined) of same signals received with ME LCTs and MB stubs, and passed to the MS;
- BC0 – an OR (or some other Boolean function => to be determined) of same signals received with ME LCTs and MB stubs and passed to the MS;
- TBIN Num – data block time bin number
- VT – valid track bit

Note that RPC track stub IDs are not implemented at this time. They will be implemented in future versions.

5. Event Record Trailer

The Event Record Trailer consists of two 64-bit words, where the most significant hex digit in each 16-bit word is the legacy DDU Code word 0xF and 0xE. Green cells in Table 9 show SP-specific configuration settings, tan cells carry the SP-specific status, yellow cells are spare.

Table 9: Event Record Trailer

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0xF				DD/CSR LF [3:0]				L1A [7:0]								TR1a
0xF				DD/CSR LF [7:4]				LFFF	0x7			0xF				TR1b
0xF				0	0	0	BB	DD/CSR BID [7,15:8] YY [3:0]				[7,15:8] MM [3:0]				TR1c
0xF				SP/CSR SCC [11:0]												TR1d
0xE				0							DD/CSR BID [4:0] DD [4:0]					TR2a
0xE				SP LADR [3:0]				SP ERSV [2:0]				SP PADR [4:0]				TR2b
0xE				LP	CRC-22 [10:0]											TR2c
0xE				HP	CRC-22 [21:11]											TR2d

Here:

- L1A [7:0] – Event Number, lower byte, same as HD1a [7:0];
- DD/CSR_LF [7:0] = 0…255 – L1A FIFO word count. Shows the L1A queue size at the moment of transmitting TR1a;
- LFFF = DD/CSR_LF[15] – L1A FIFO Full Flag (LF word count = 256) at the moment of transmitting TR1a;
- DD/CSR_BID [7] = {BB} – SP readout configuration year base (0 / 16)
- DD/CSR_BID [15:8] = {YY [3:0], MM [3:0]} – SP readout configuration year (2000 + 16*BB + YY) and month (MM);
- DD/CSR_BID [4:0] = DD [4:0] – SP readout configuration day;
- SP/CSR_SCC [11:0] – SP Core Configuration Register;
- TR2b == HD2b;
- LP – Low Parity => Even Parity bit for CRC-22 [10:0]
- HP – High Parity => Even Parity bit for CRC-22 [21:11]
- CRC-22 [21:0] – the last 4 Event Record Trailer words are not included in the CRC

Revision history

Date	Notes
2014-07-15	Converted from Lev Uvarov's specification of the legacy DAQ format: http://www.phys.ufl.edu/~uvarov/SP05/LU-SP2DDU_Event_Record_Structure_v53.pdf Significantly reworked to adapt the format for MTF7. This is an initial draft; it will be modified in the future.
2014-07-21	SP output data record reworked to allocate more bits for track segment IDs. Each track stub ID is now a 5-bit value.
2015-03-18	Removed RPC enable flags from header for now. Made ME enable flags longer to accommodate chabmers from neighbor sector.
2015-10-09	Increased ME1_ID field length to 6 bits, to accommodate both subsectors + track stub number Added VT bit (valid track)
2015-12-03	Fixed errors in Table 8, added GMT track parameters to output Removed FMM section copied from DAQ document
2016-03-15	Added better explanation to MEx_ID and Quality fields in SP Output data record