IT-μDTC firmware development
Simulation and testing of RD53A Chip Readout with FC7

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IT-μDTC Firmware Blocks Integration

- DIO5, AMC 13, TTC Decoder Blocks and IPBus register types are inherited from the d19c-firmware
- I will remove the unused OT specific parts from the firmware and port the new and modified blocks
- Brand new and modified blocks will need new IPBus slaves and register addresses
- Gitlab project for the firmware integration → https://gitlab.cern.ch/tbalazs/IT-uDTC-firmware

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DIO5, AMC 13 and TTC Decoder Blocks

- distributes commands, trigger and clock to the AMC boards of the uTCA crate
- information generated externally or internally like TCDS
- TTS information is accessible remotely

- FMC card
- external clock
- external trigger

- Clock and orbit signals derived from the LHC RF system come to the P5 TTC machine interface
RD53A Chip Simulation

- The RD53A chip simulator is written in Verilog and SystemVerilog
- Some features of SystemVerilog are still not supported even in the newest Vivado release
- 3rd party simulators like Questa and ModelSim are able to run these simulations
- The best solution would be to call the 3rd party simulator from Vivado directly
- The chip simulator is an effective tool for debugging firmware blocks