IT-µDTC firmware development
Simulation and testing of RD53A Chip Readout with FC7

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RD53A Heartbeat Signal Readout

- Aurora receiver needs external 160MHZ clock
- Low jitter clock is generated by PLL in CERN and KSU FMC
- PLL is programmed by I2C → I2C needs to be ported to the firmware

- I2C FSM implemented by Russell is ported to firmware with the help of Alex
- PLL reset pin is connected to FPGA fabric from the FMC
- Default state is high → active low trigger reset
- Firmware needs to keep signal at high

Q: Do we want this at fix value or define reset separately to FMC or is there a firmware system reset to connect to?

- How does bdaq53 treats reset? Is there an individual reset for the FMC?
- How does OT d19c treat reset?
- Idea: Should we implement the same way as in bdaq53 for need to better align with the middleware?
RD53A Heartbeat Signal Readout

- Verified clock module with hardware by
  → checking clock with LED blinking
  → comparing 10MHz clock to 320MHz clock
- Working on simple check to measure ratio of 320MHz clock and 160 MHz clock from FMC fabric

Currently the PLL is programmed in 4 steps
- **step 1**: set PLL reset to high
- **step 2**: set fmc power on
- **step 3-4**: set I2C high and set I2C low