IT-μDTC firmware development
Simulation and testing of RD53A Chip Readout with FC7

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Supported by OTKA K124850
RD53A Heartbeat Signal Readout

Hardware-related section

- Plugging CERN FMC to L12 in FC7
  → PLL is programmed and the fpga clock checked
  → Alex found that SY58608U chip's input is DC-coupled not AC-coupled by default
  → we have bypassed the 100nF capacitors in CERN FMC
  → PLL configuration should probably be modified
    → set the common mode of the PLL output to 1.2 V
    → set VDDO for PLL to 3.3V with J8 jumper in CERN FMC (suggested by Alex)

- Plugging CERN FMC to L8 in FC7
  → gbt clock will be AC-coupled by default in the same way as in case of KC705
  → when CERN FMC plugged in to the L8 connector FC7 not able to power up correctly
    → current consumption decreased from 1 A to 750 mA
    → green power LEDS did not flash on and golden firmware not loaded
  → even after plugging in the CERN FMC after startup gives the same results (suggested by Luismi)

Firmware-related section

- IT-uDTC-firmware is forked
- IT firmware project is built up to system core
- IT user core or OT user core ??
- we will try to update on Monday or Tuesday