IT-µDTC firmware development
Simulation and testing of RD53A Chip Readout with FC7

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Supported by OTKA K124850
IT-µDTC Firmware Development Update

- Running development tasks in order
  - Porting DIO5 ➔ **Ready**
    - i2c multi-master problem with CERN or Kansas FMC ➔ **need to be solved**
  - Porting TLU ➔ **To do**
  - Porting AMC13 ➔ **To do**
  - Porting TTC Decoder ➔ **To do**

Porting DIO5 FMC to the IT-firmware

- Overview and summary
  - pin assignment for DIO5 is made according to the **EDA-02408-V2-0** DIO5 schematic
  - schematic and pin assignment is uploaded to the DAQ site: [https://espace.cern.ch/Tracker-Upgrade/DAQ.SitePages/Home.aspx](https://espace.cern.ch/Tracker-Upgrade/DAQ.SitePages/Home.aspx)
  - constraints for DIO5 are created for both L8 and L12 FMCs

Porting TLU to the IT-firmware

- Overview and motivation
  - Input 2 and 5 in DIO5 are used for external triggering and external clock source
  - Inputs 1,3 and 4 in DIO5 can run the TLU’s clock, busy and reset signals
  - routing is necessary to both fast command and command processor blocks
  - bufgmux modification is necessary in the clock generator block in case of ext clk of DIO5
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Porting CERN FMC to the IT-firmware

- Overview and necessary modifications
  - currently only a few signals are used
  - pin assignment is created to port all the signals
  - new records can be created in \texttt{IT_user_package_basic.vhd} like in all other cases

Porting KANSAS FMC to the IT-firmware

- Overview and motivation
  - revision of the aurora records in \texttt{user_package_basic.vhd} is necessary for routing all the lanes
  - new records need to created for io and mgt signals
  - with the help of the records and pin assignment porting is straightforward

- Additional development tasks
  - 6 tcl script were created to constrain CERN, KANSAS and DIO5 FMCs for both L12 and L8 FMCs
  - Build configure script is created for both bitstream generation and FMC porting
    - FMC1 and FMC2 constants declared in the \texttt{IT_user_package_basic.vhd}
  - PLL’s output frequencies were reconfigured to 80.157MHz and 160.314MHz respectively for CERN and KANSAS FMCs to meet the needs of the LHC clock and make the system robust

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